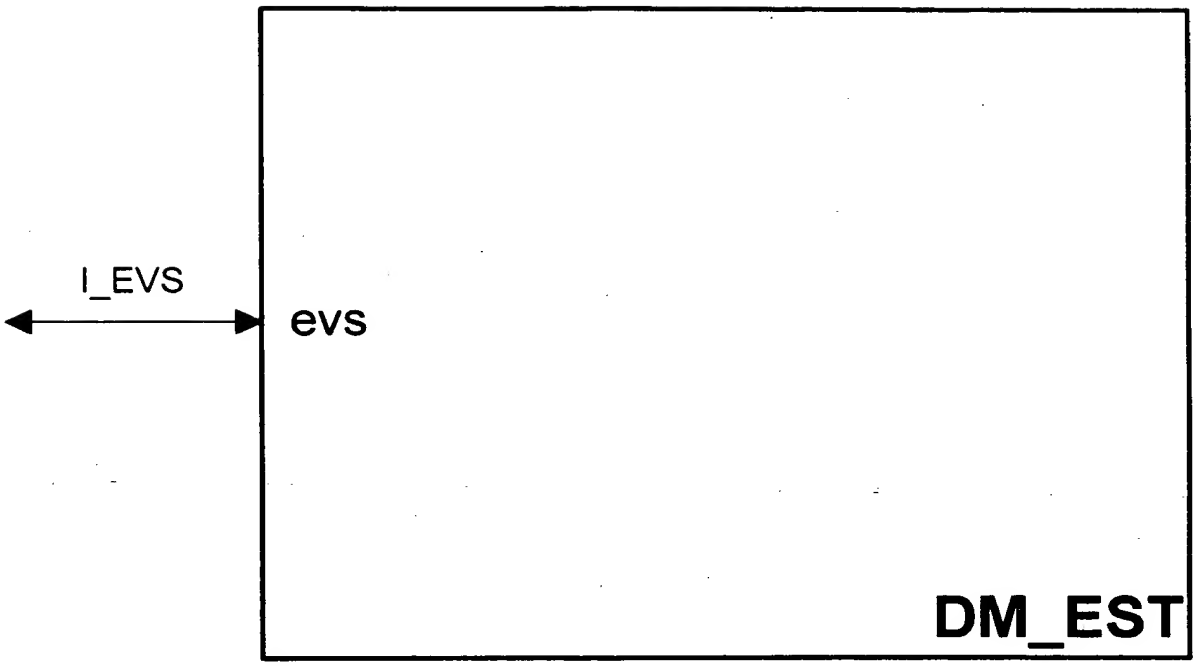


Fig. 1

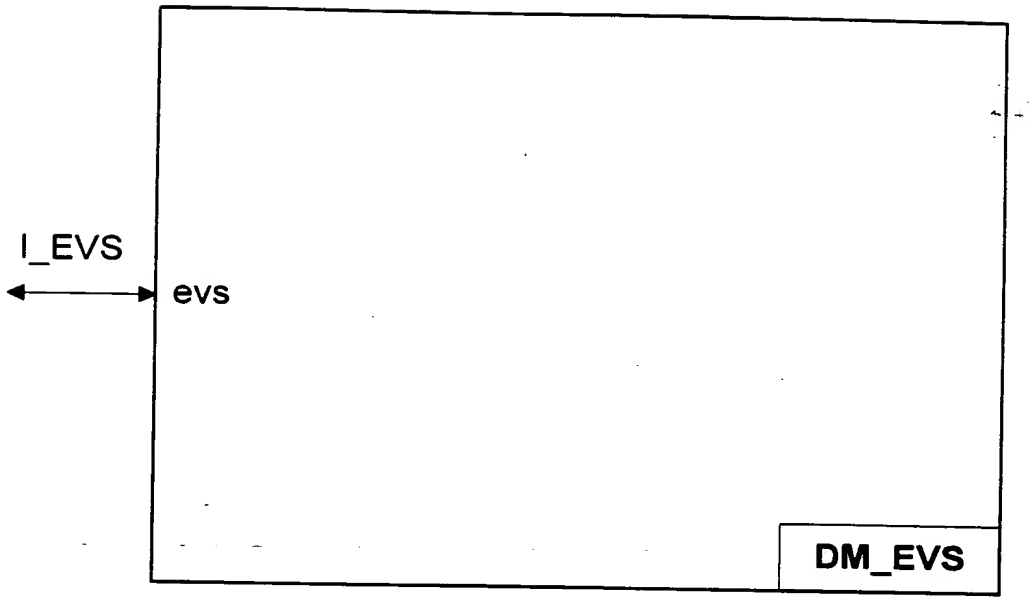


Fig. 2

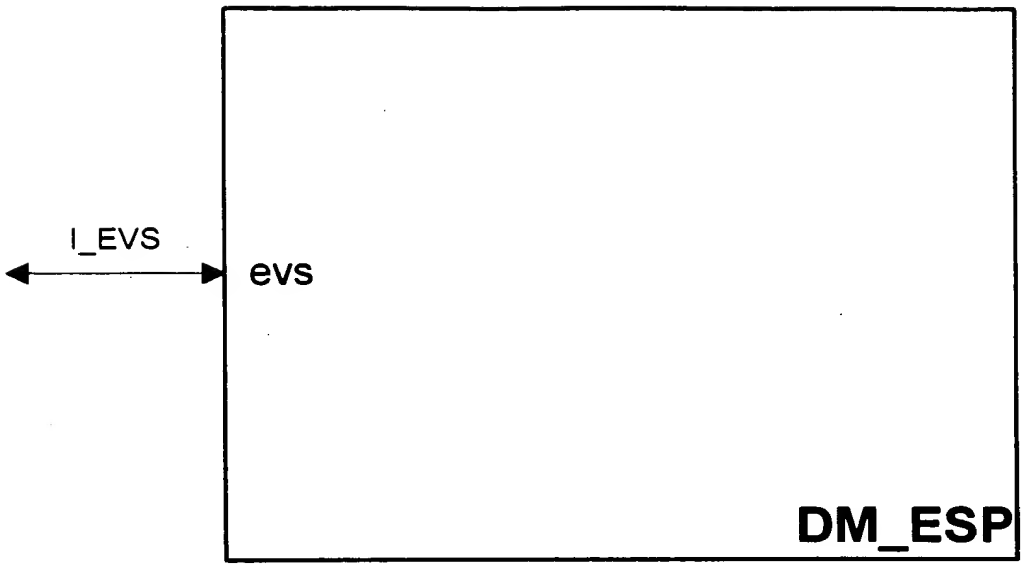


Fig. 3

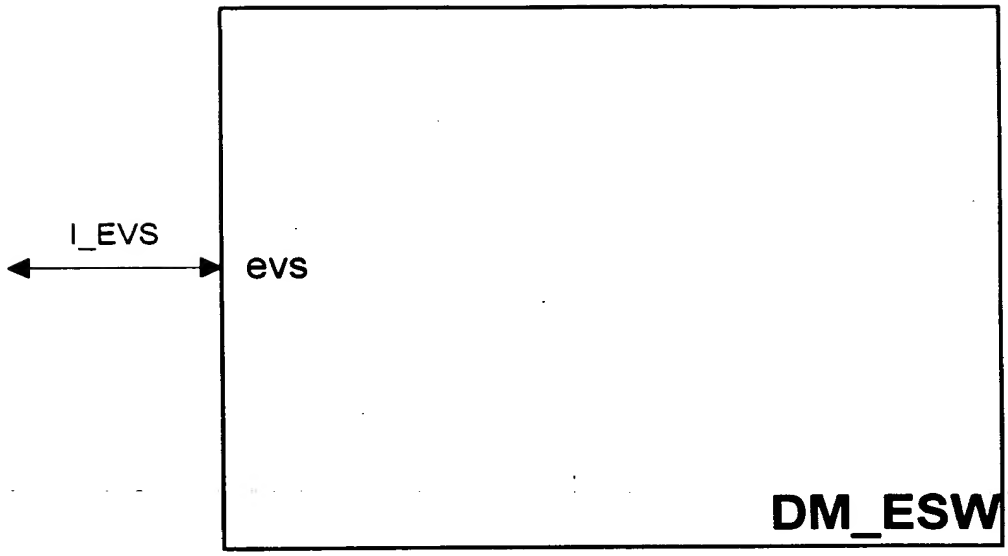


Fig. 4

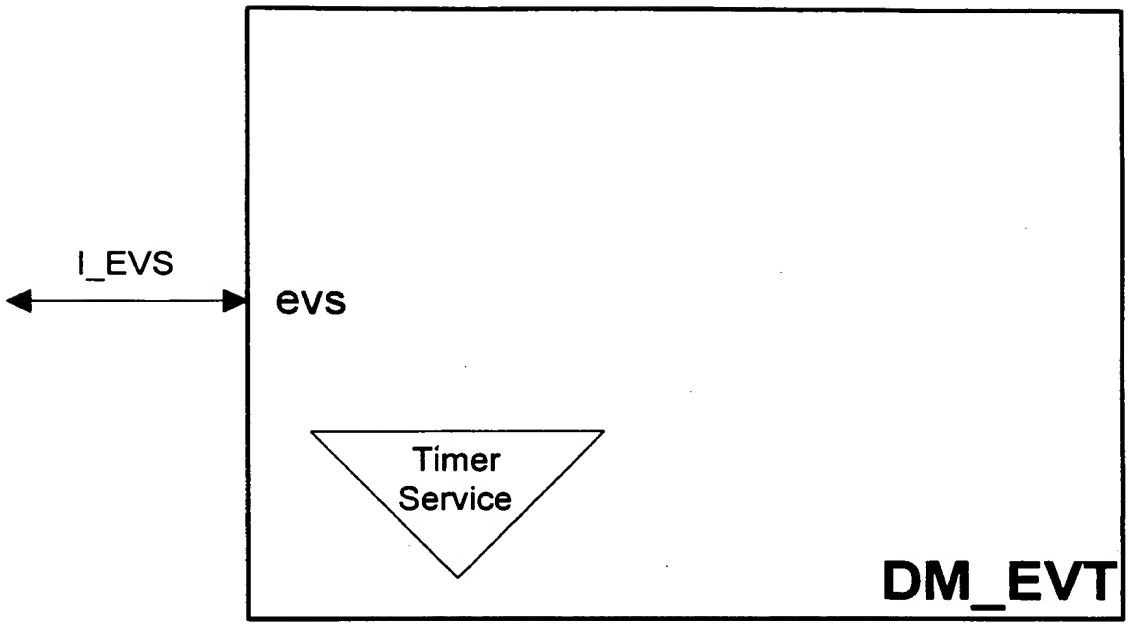


Fig. 5

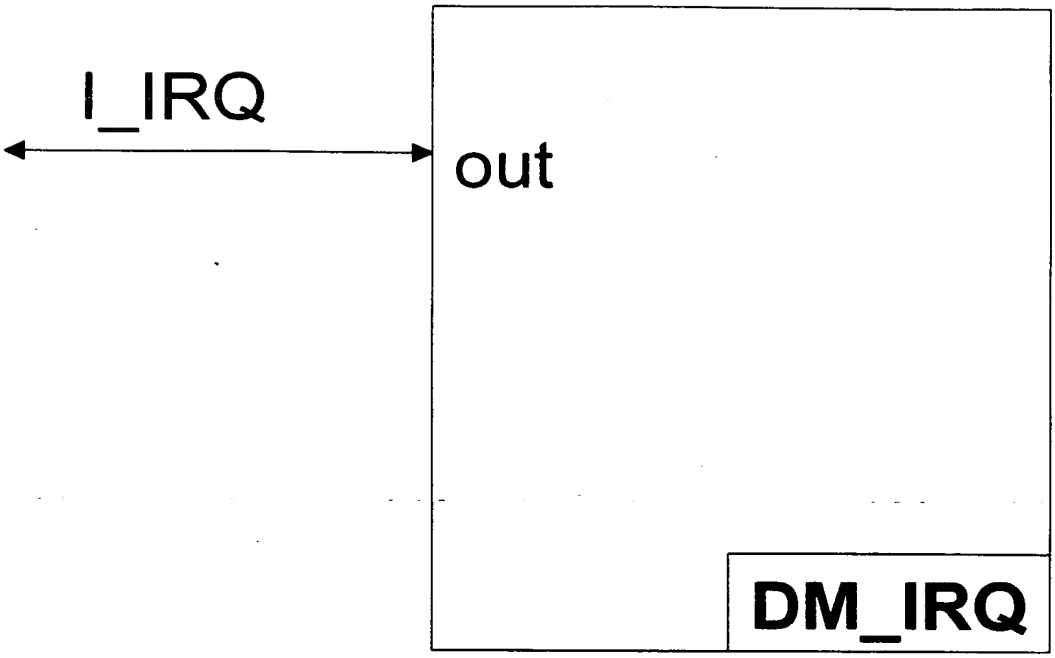


Fig. 6

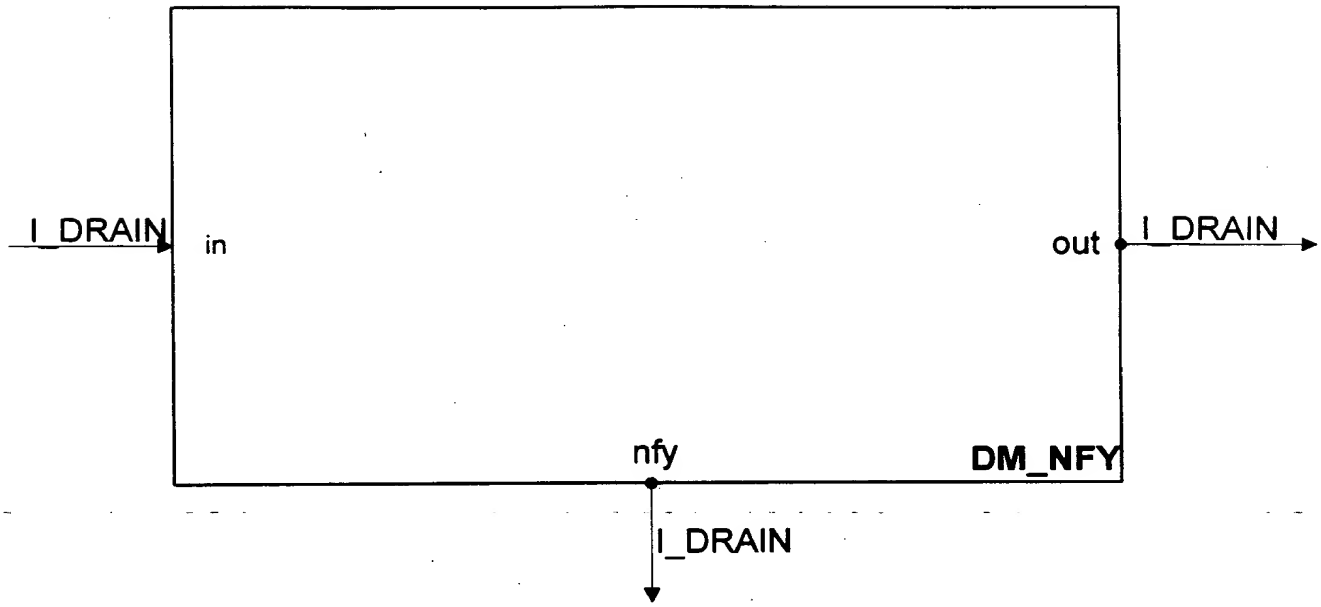


Fig. 7

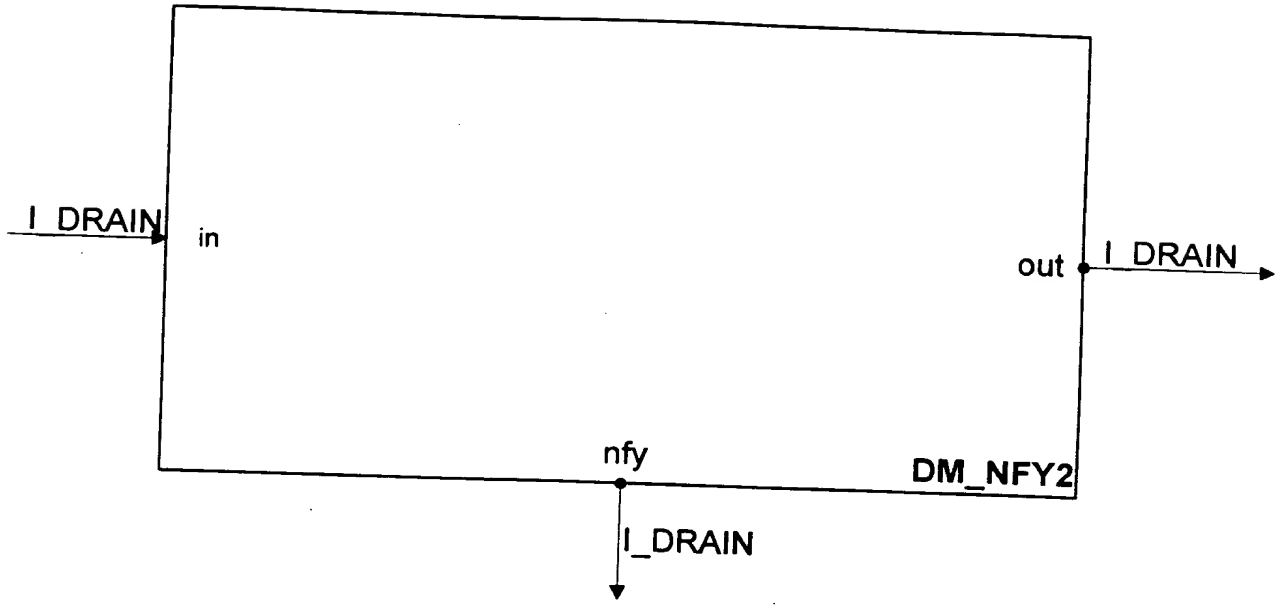


Fig. 8

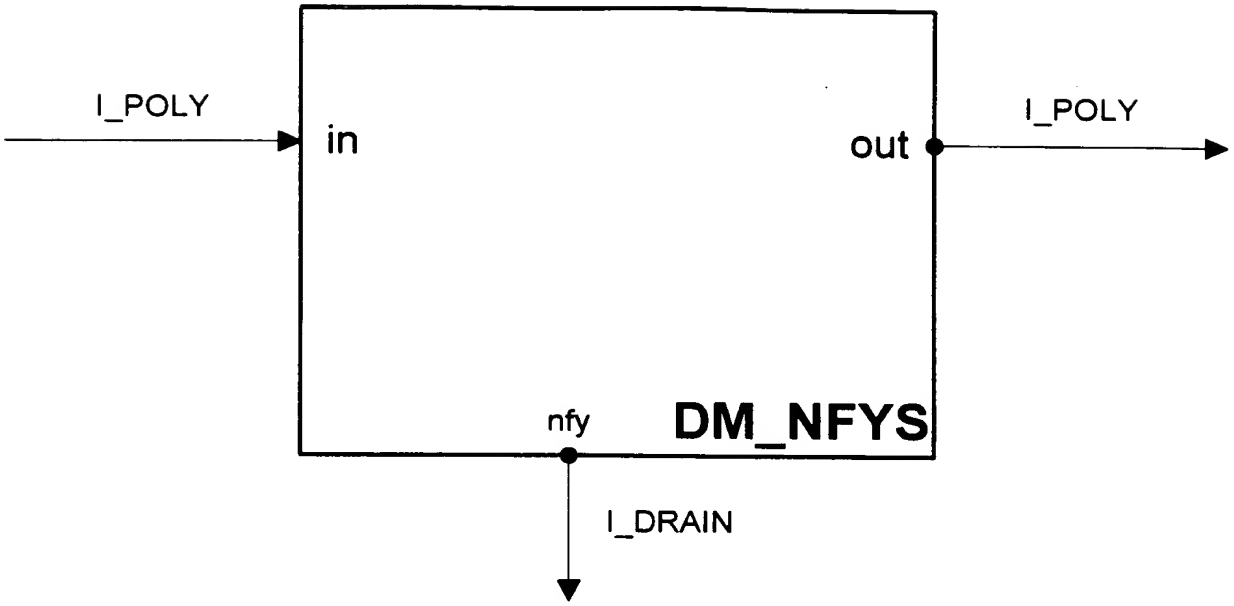
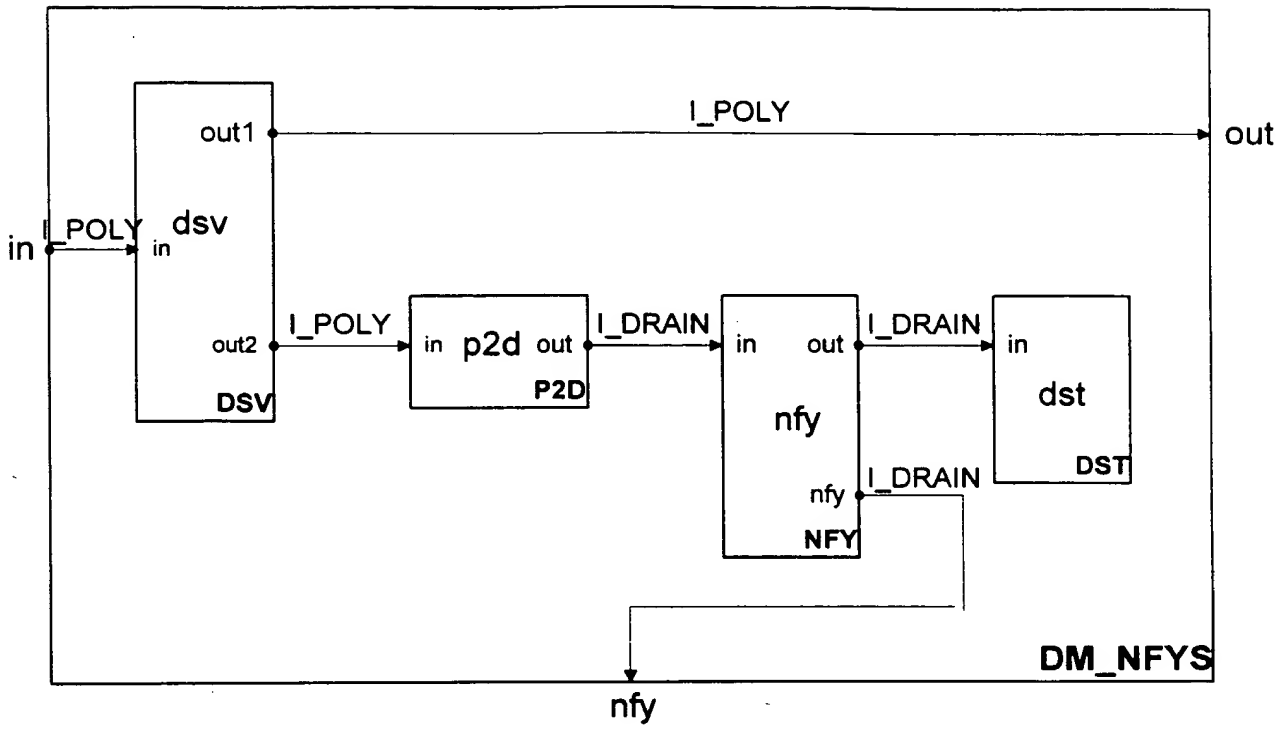


Fig. 9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out2
DSV
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out
P2D
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in
out
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in
dst
DST
nfy
I_DRAIN
DM_NFYS
nfy

Fig. 10

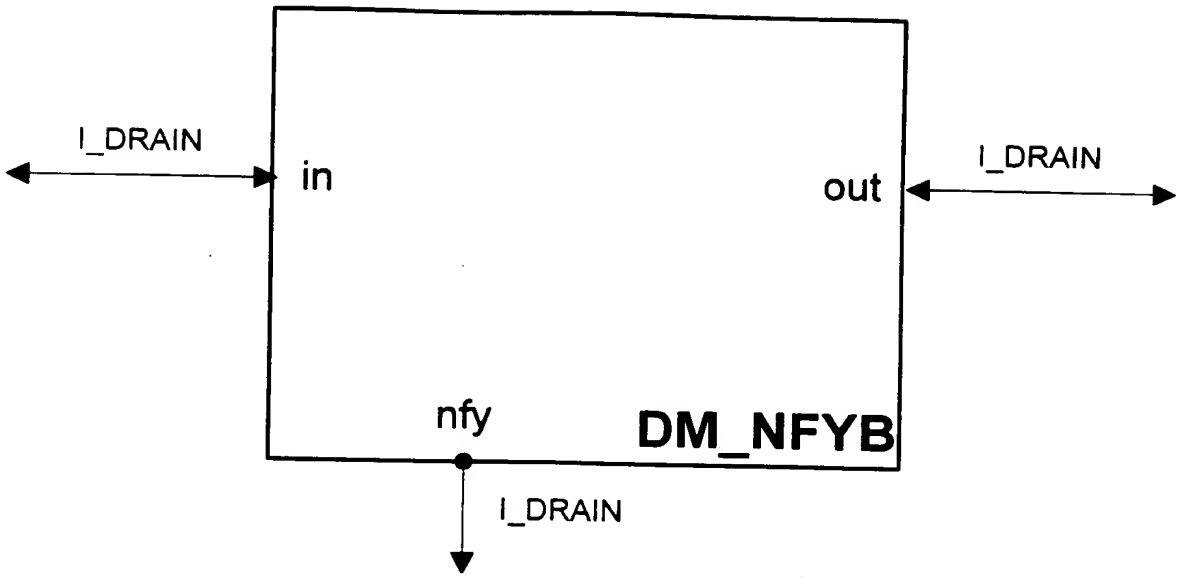
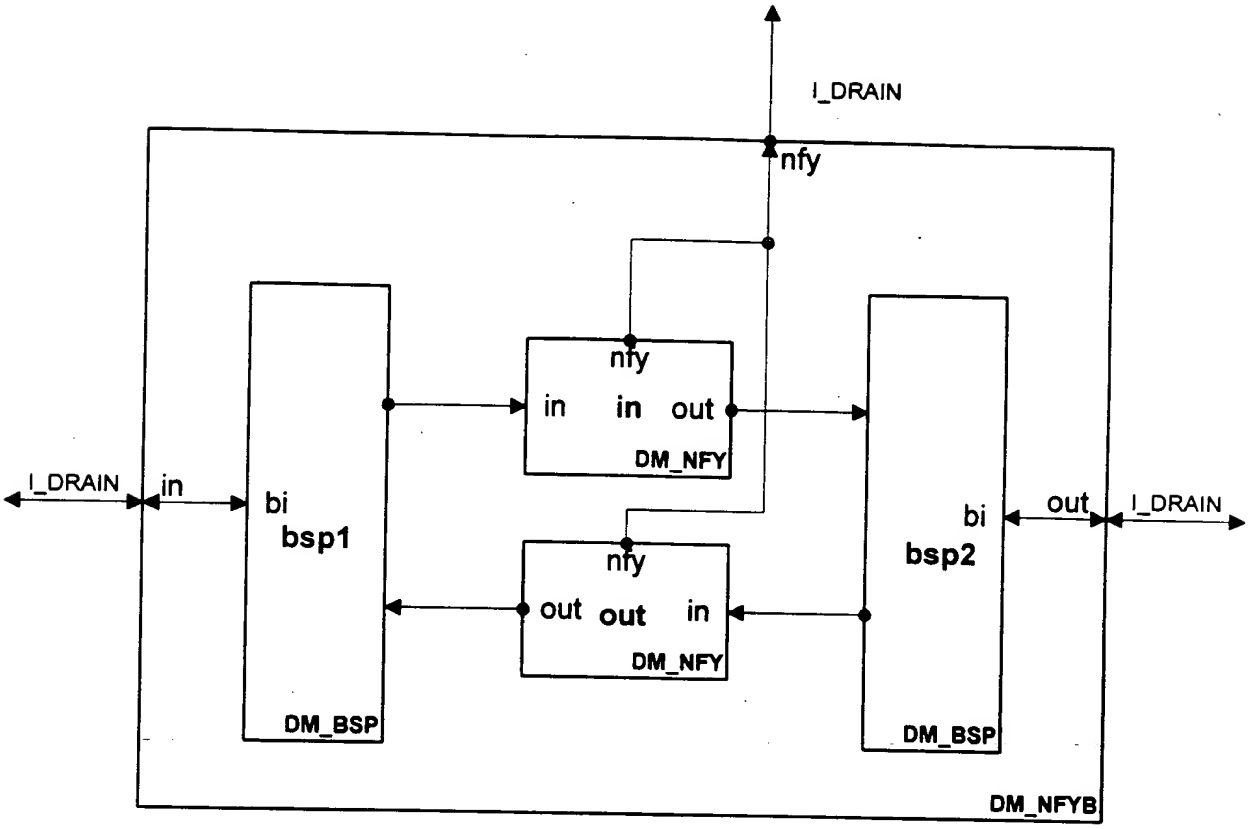


Fig. 11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bi
bsp2
DM_BSP
out
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DM_NFYB

Fig. 12

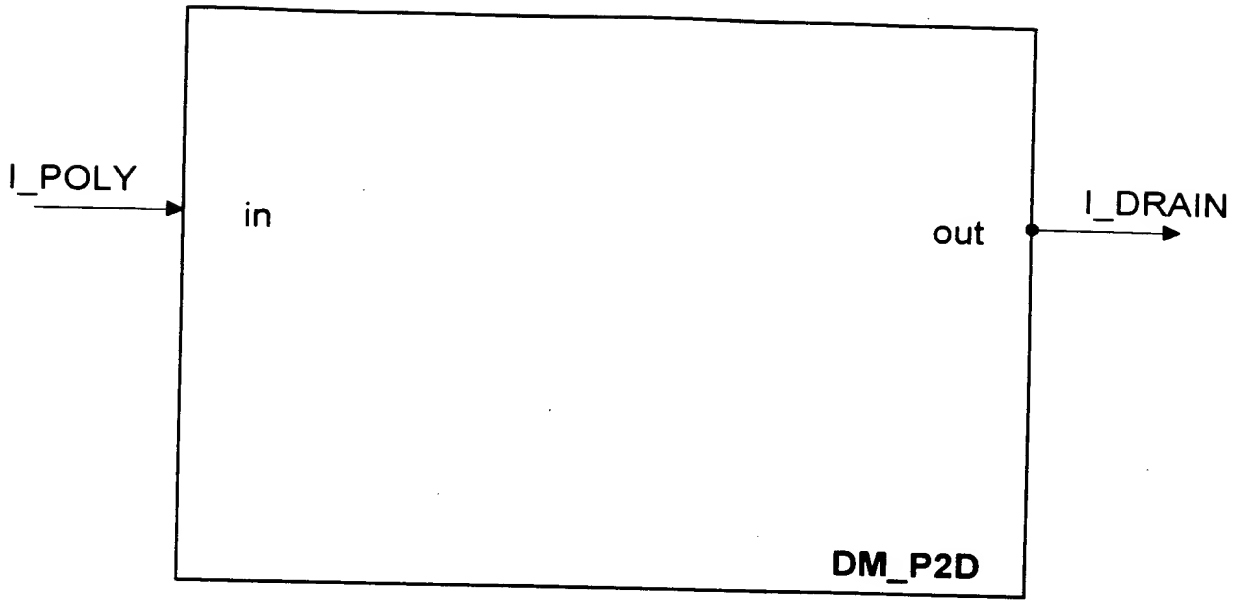


Fig. 13

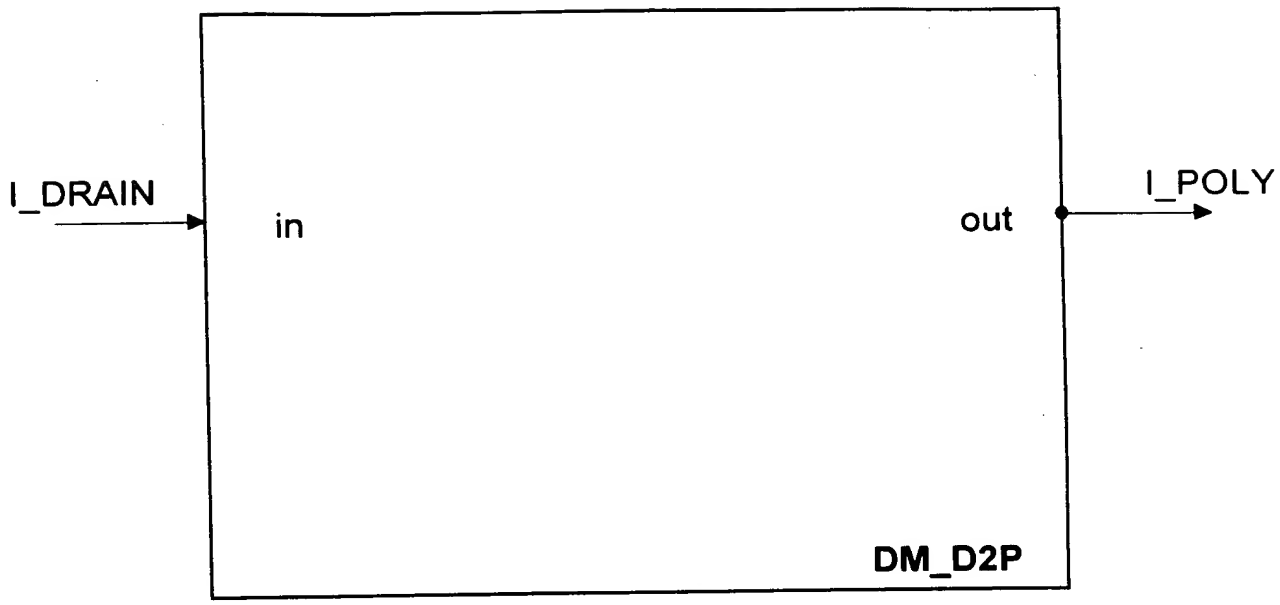


Fig. 14

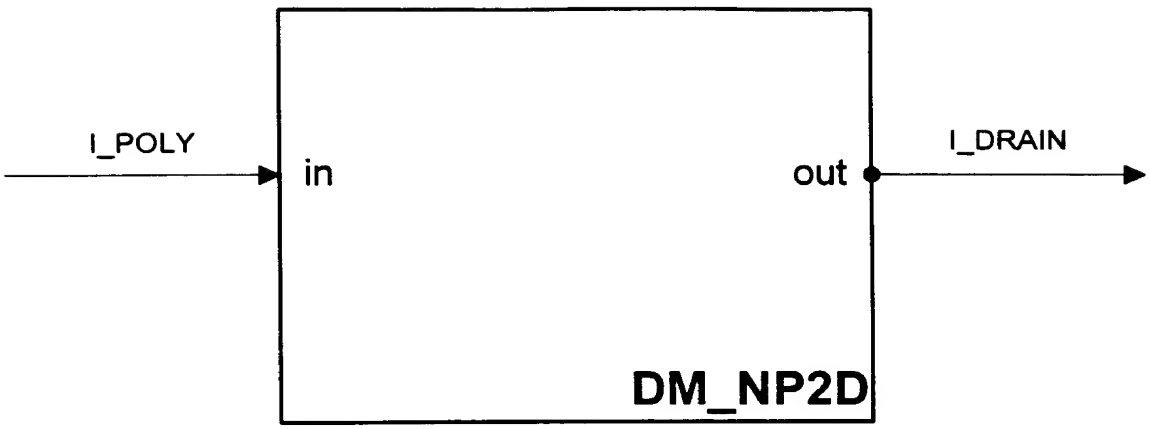


Fig. 15

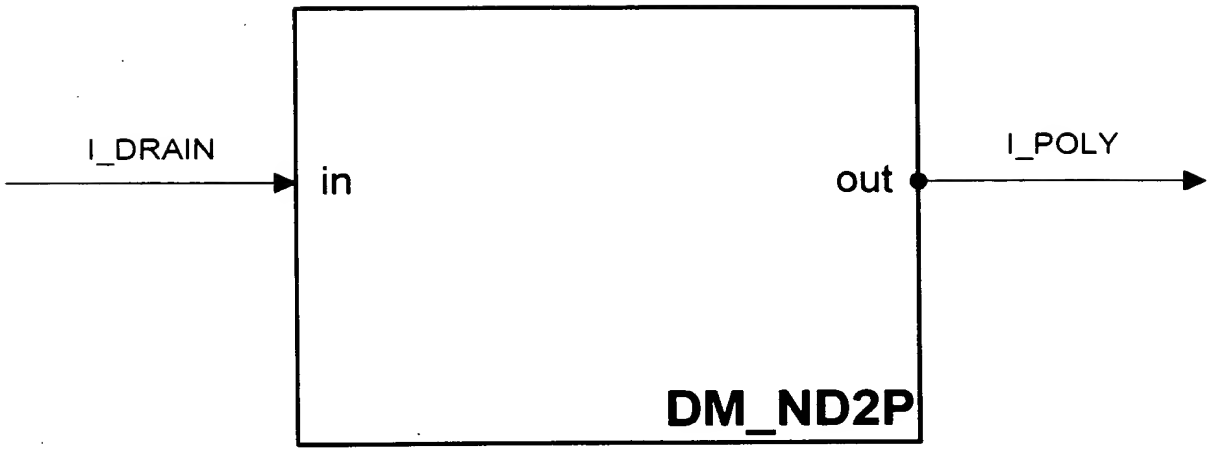


Fig. 16

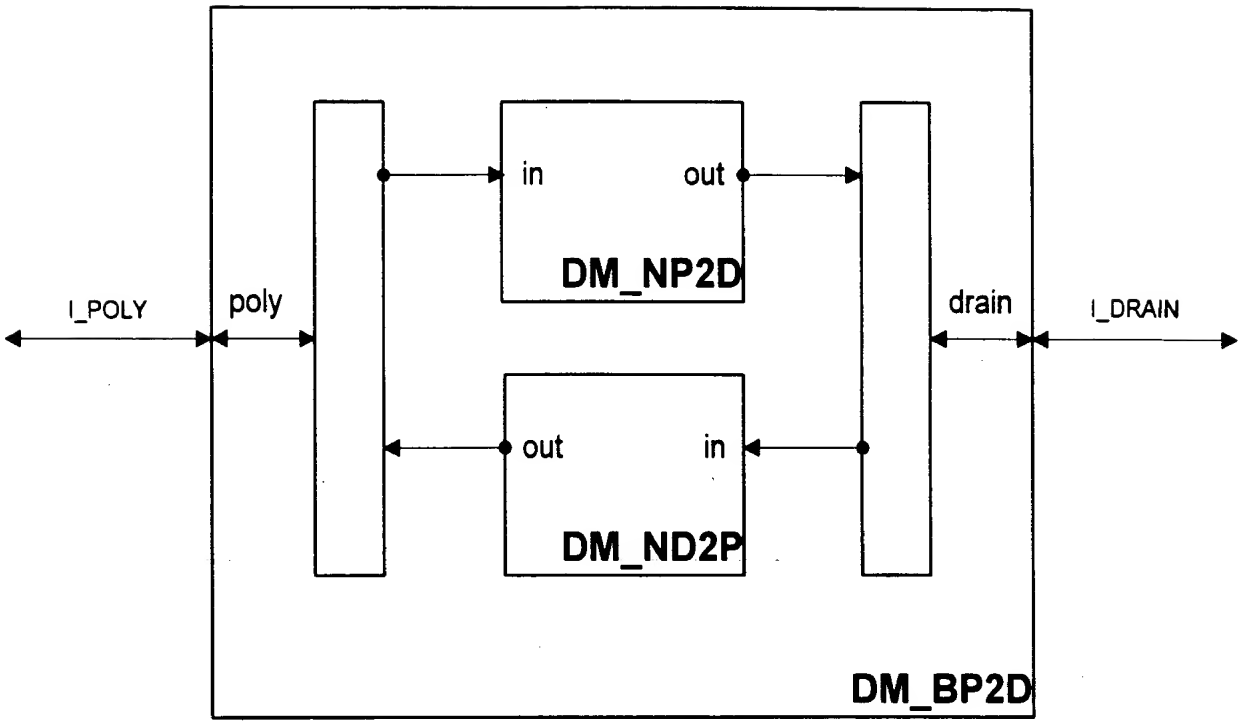


Fig. 17

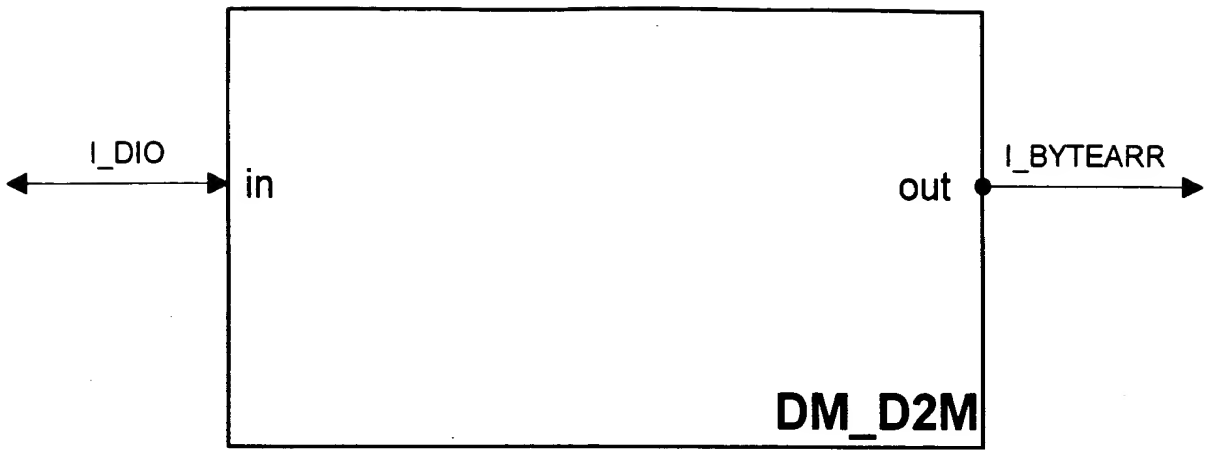


Fig. 18

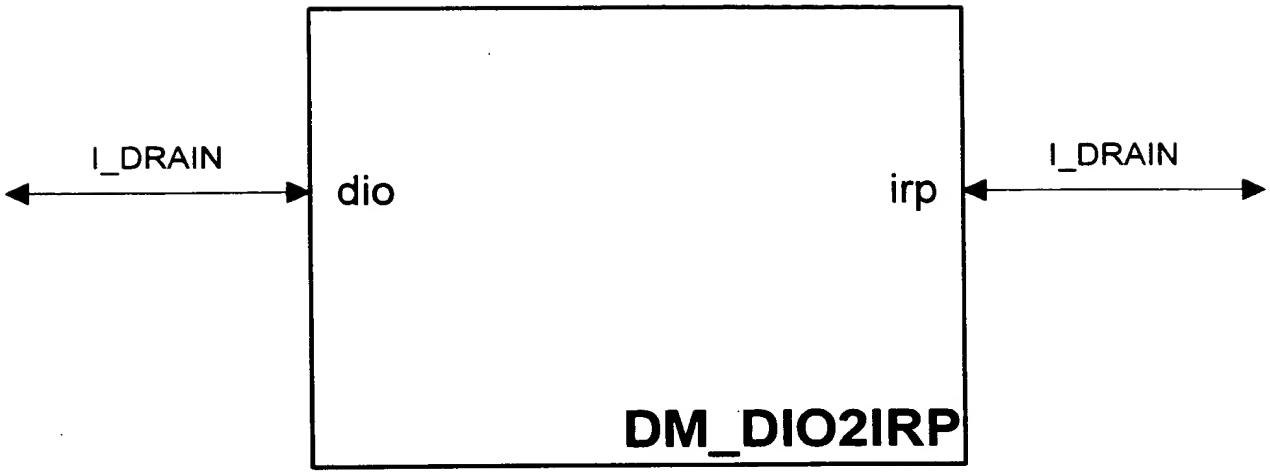


Fig. 19

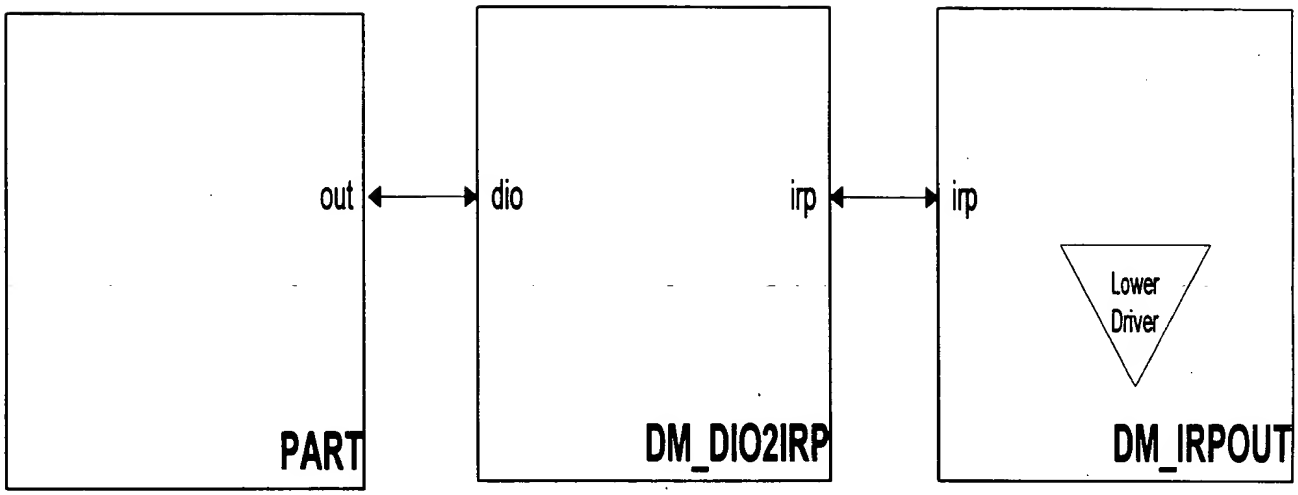


Fig. 20

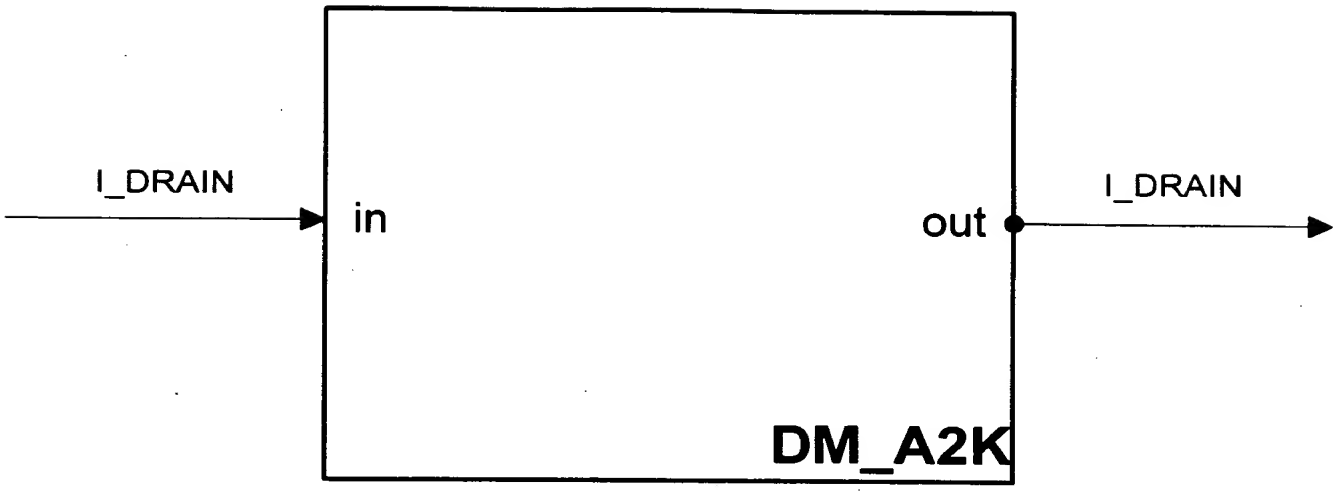


Fig. 21

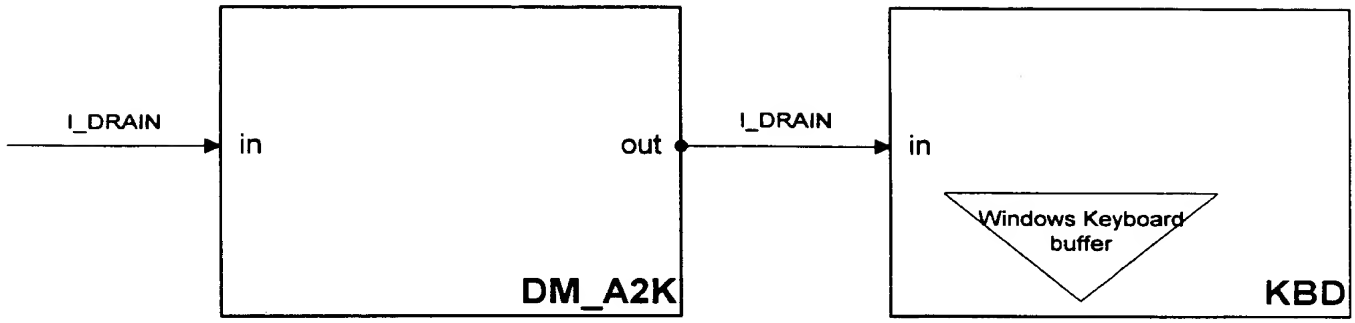


Fig. 22

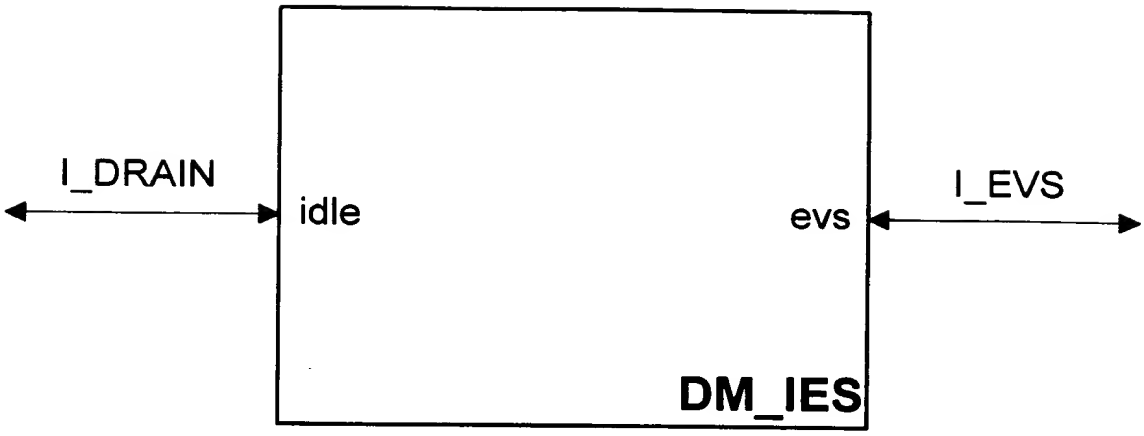


Fig. 23

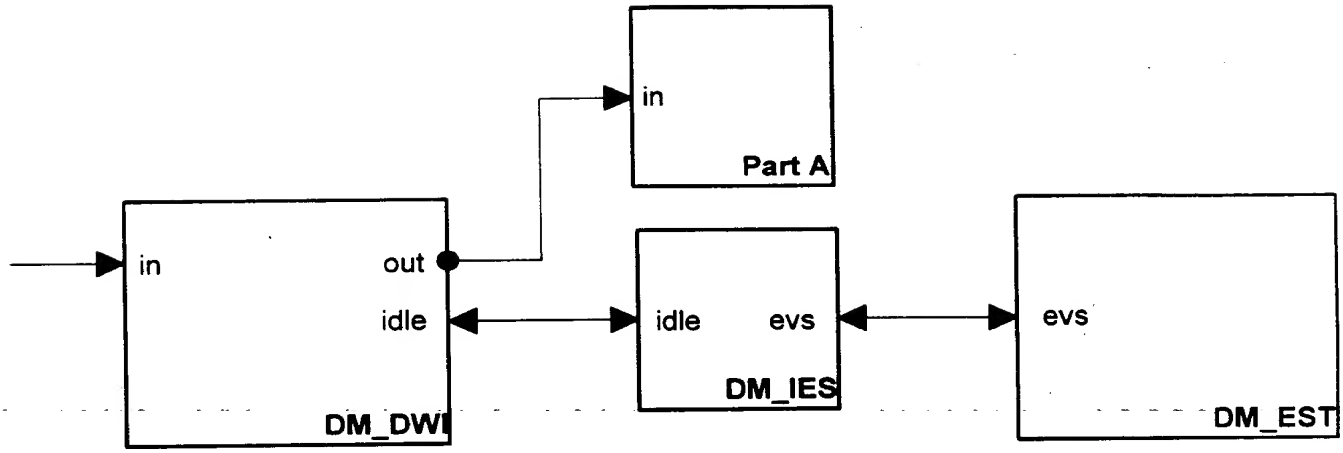


Fig. 24

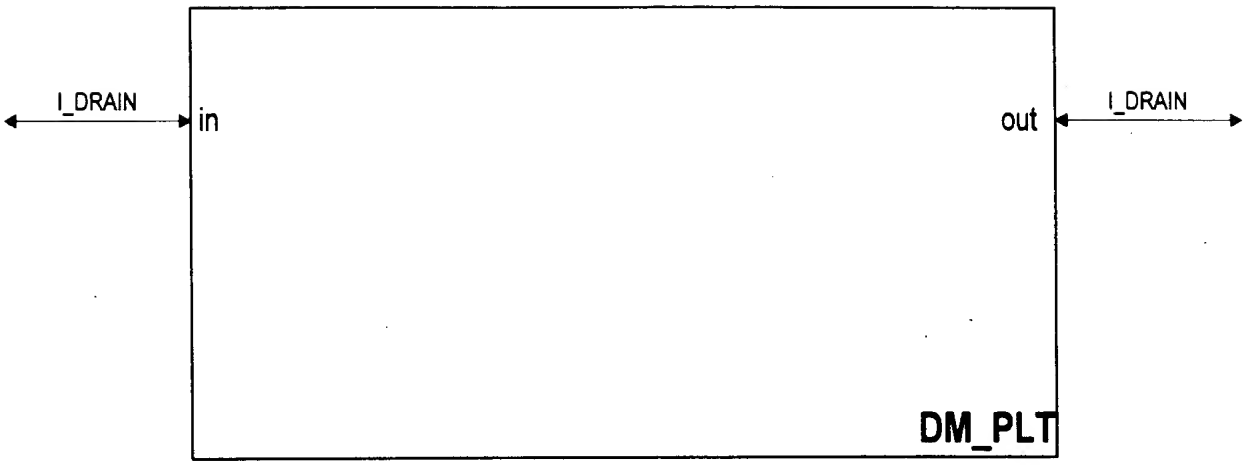


Fig. 25

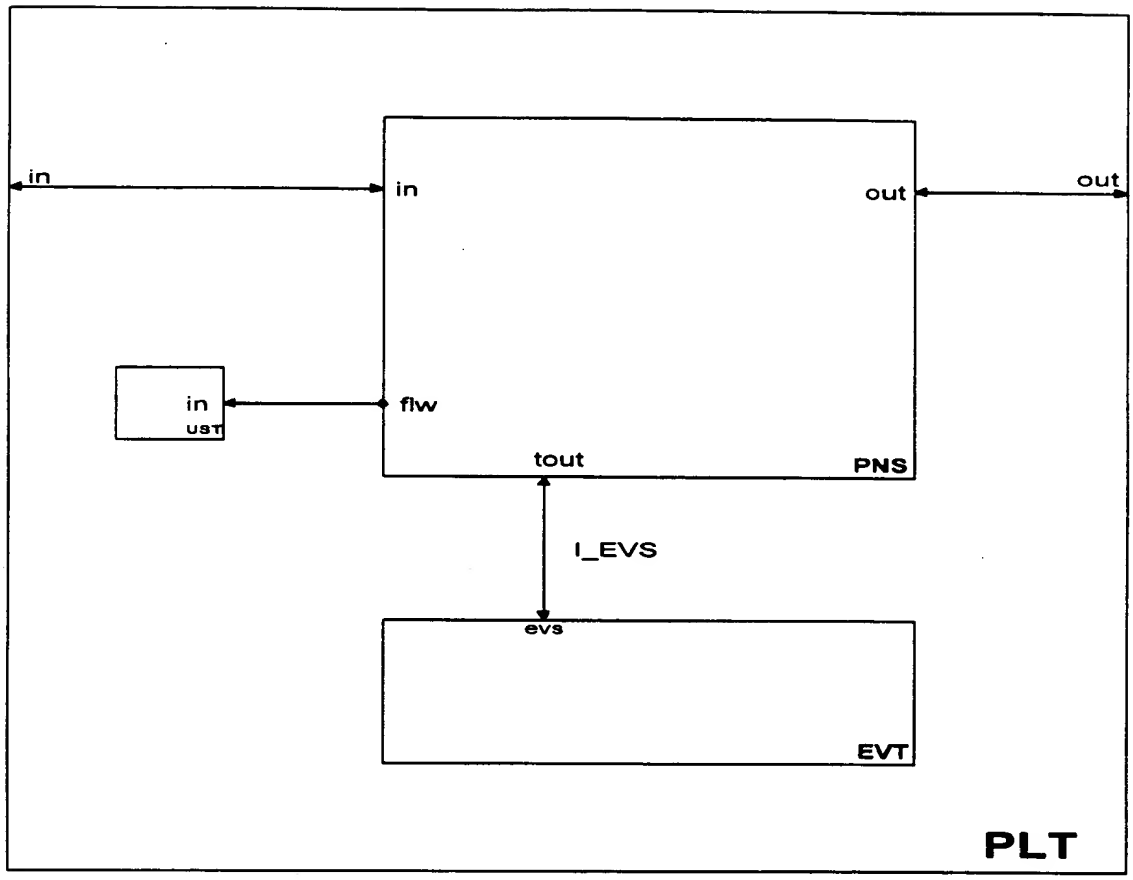


Fig. 26

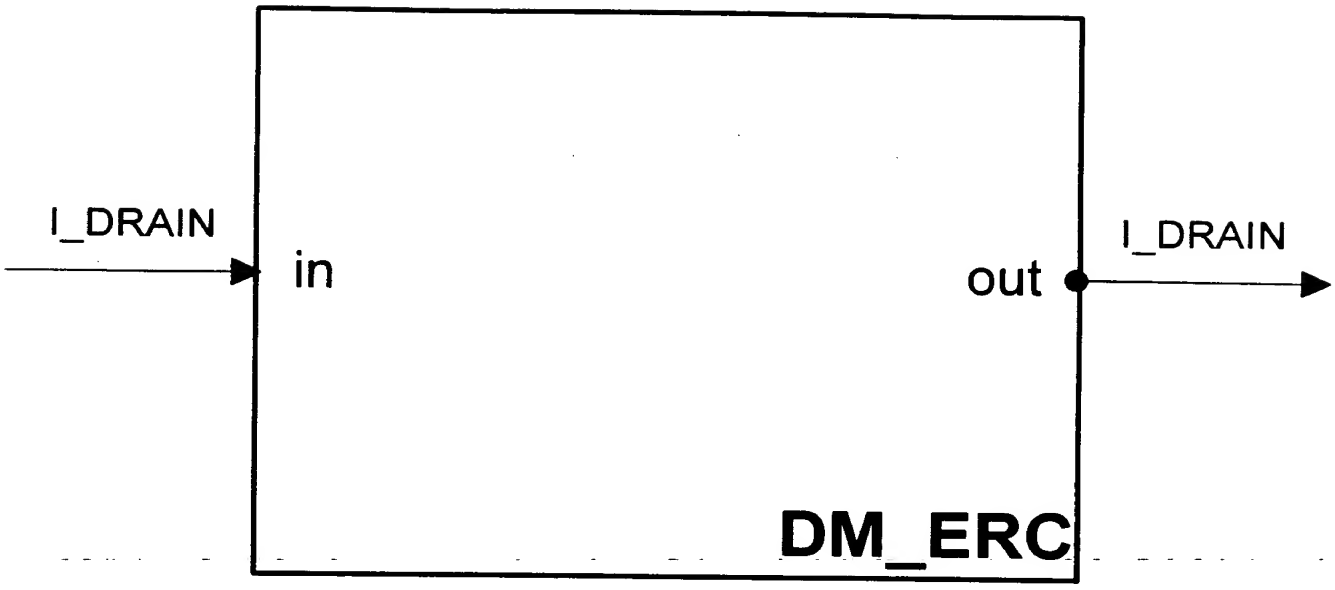


Fig. 27

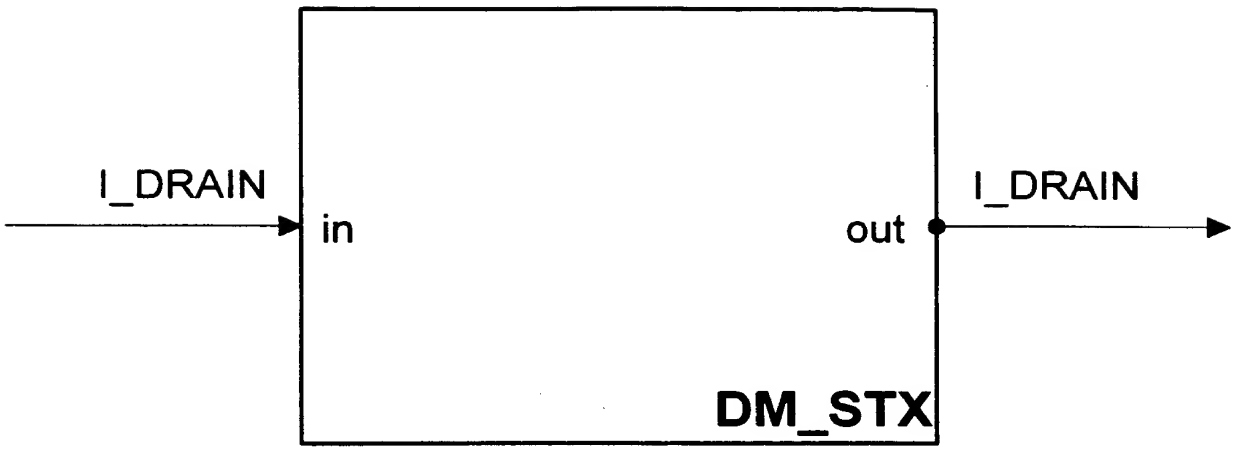


Fig. 28

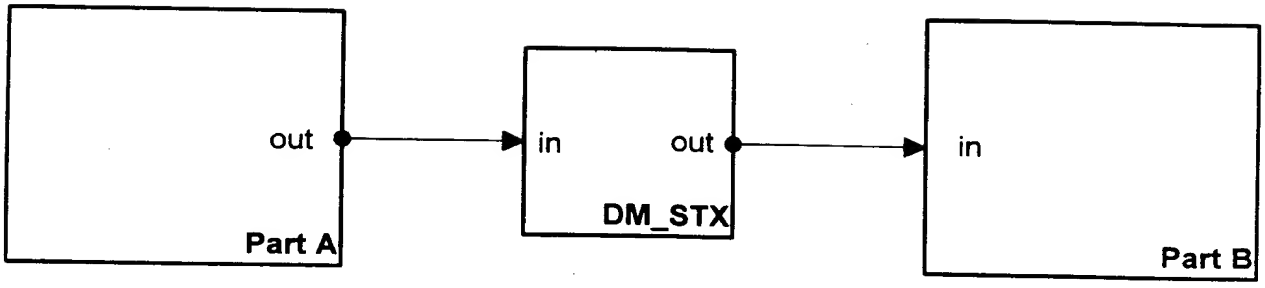


Fig. 29

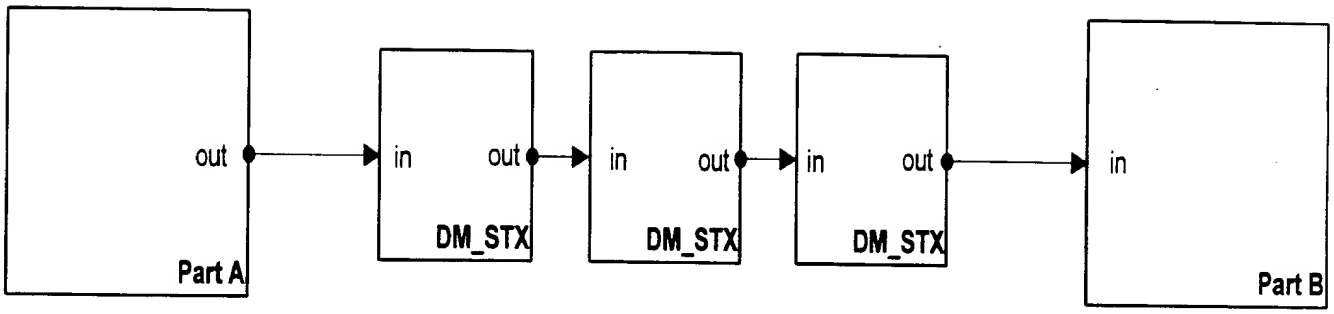


Fig. 30

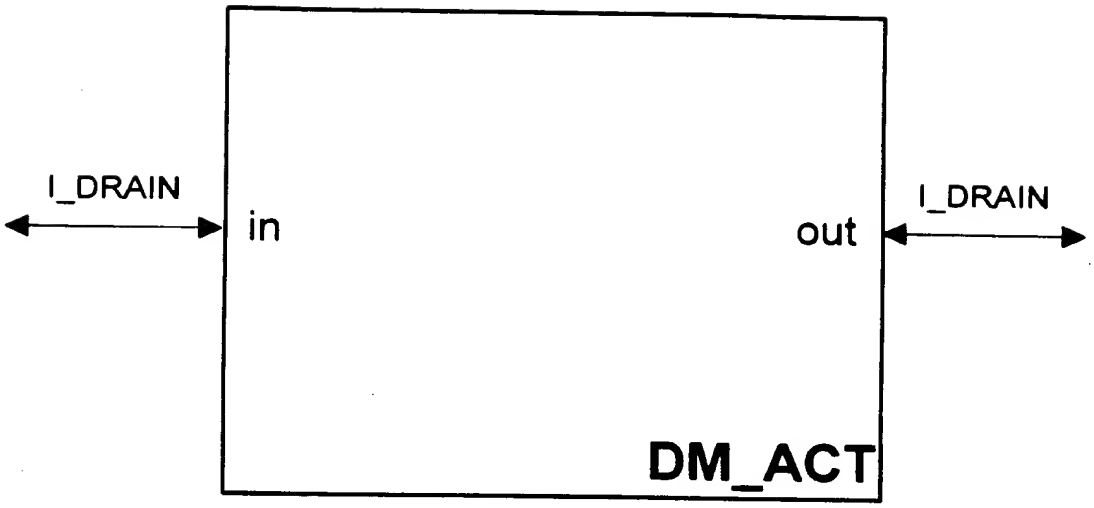


Fig. 31

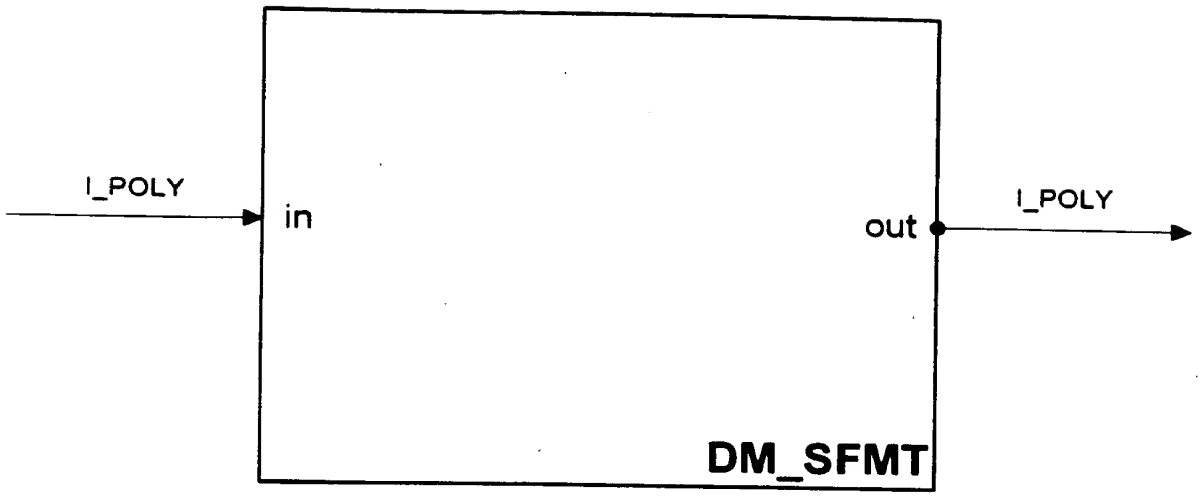


Fig. 32

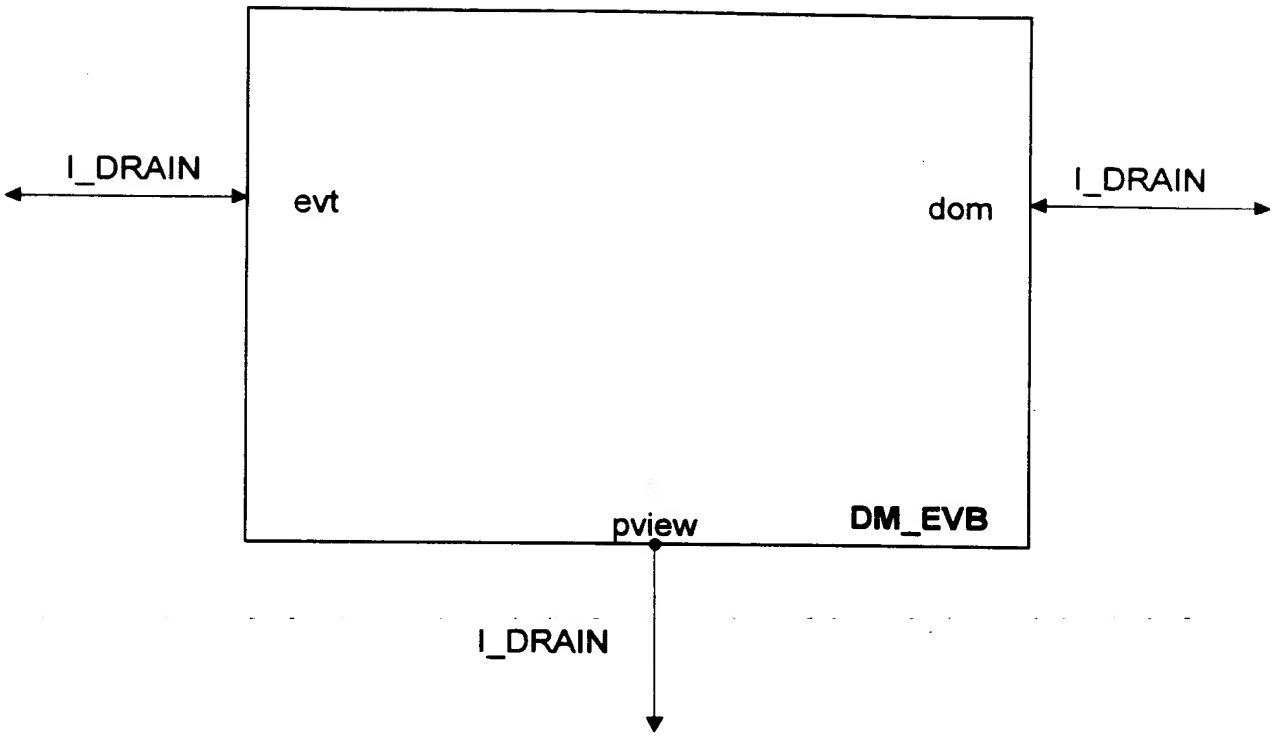


Fig. 33

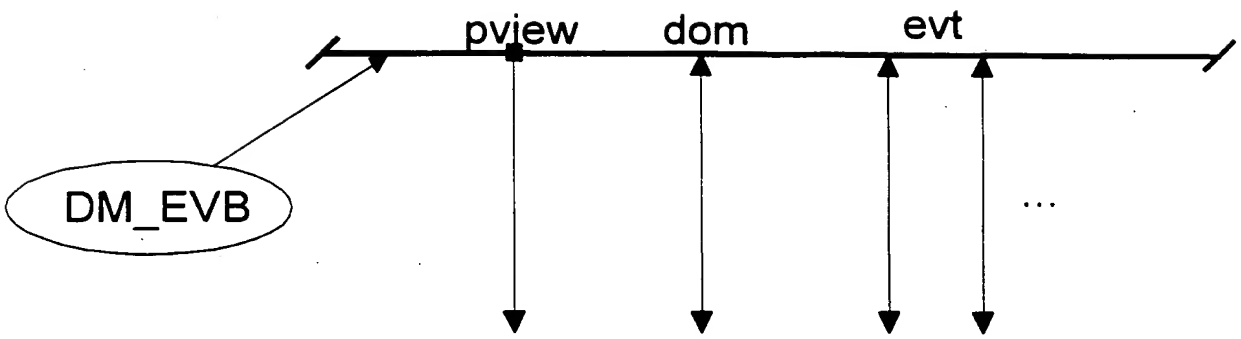
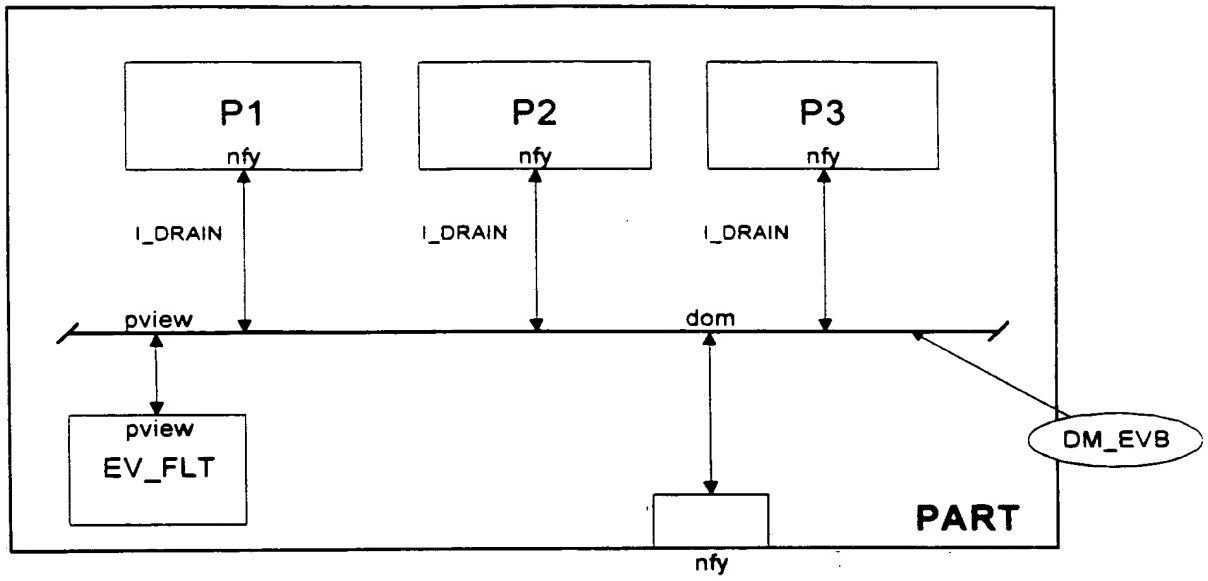


Fig. 34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P2
nfy
P3
nfy
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I_DRAIN
I_DRAIN
pview
dom
pview
EV_FLT
DM_EVB
PART
nfy

Fig. 35

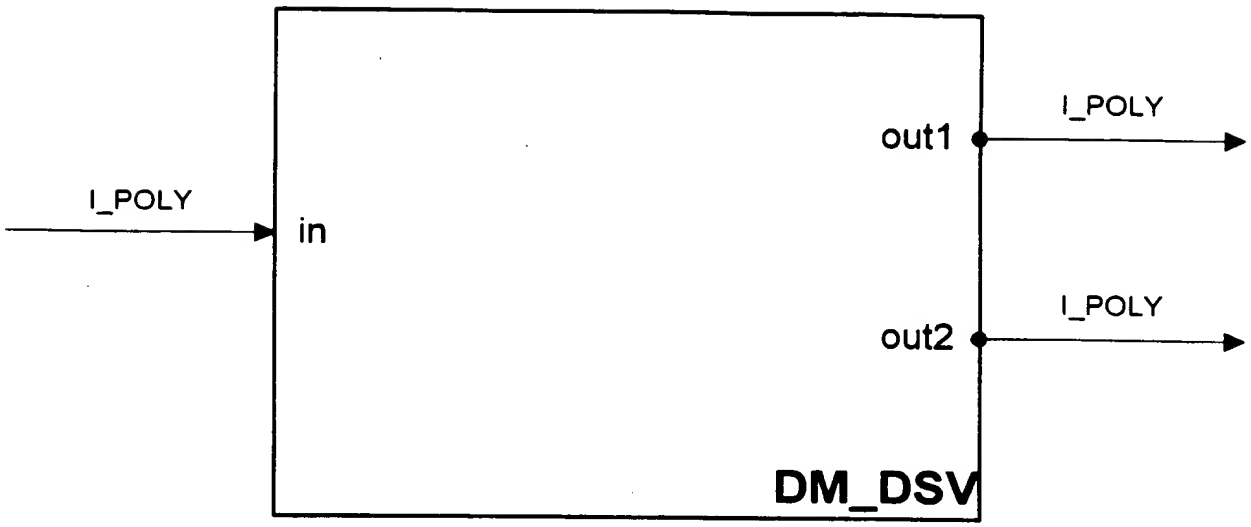
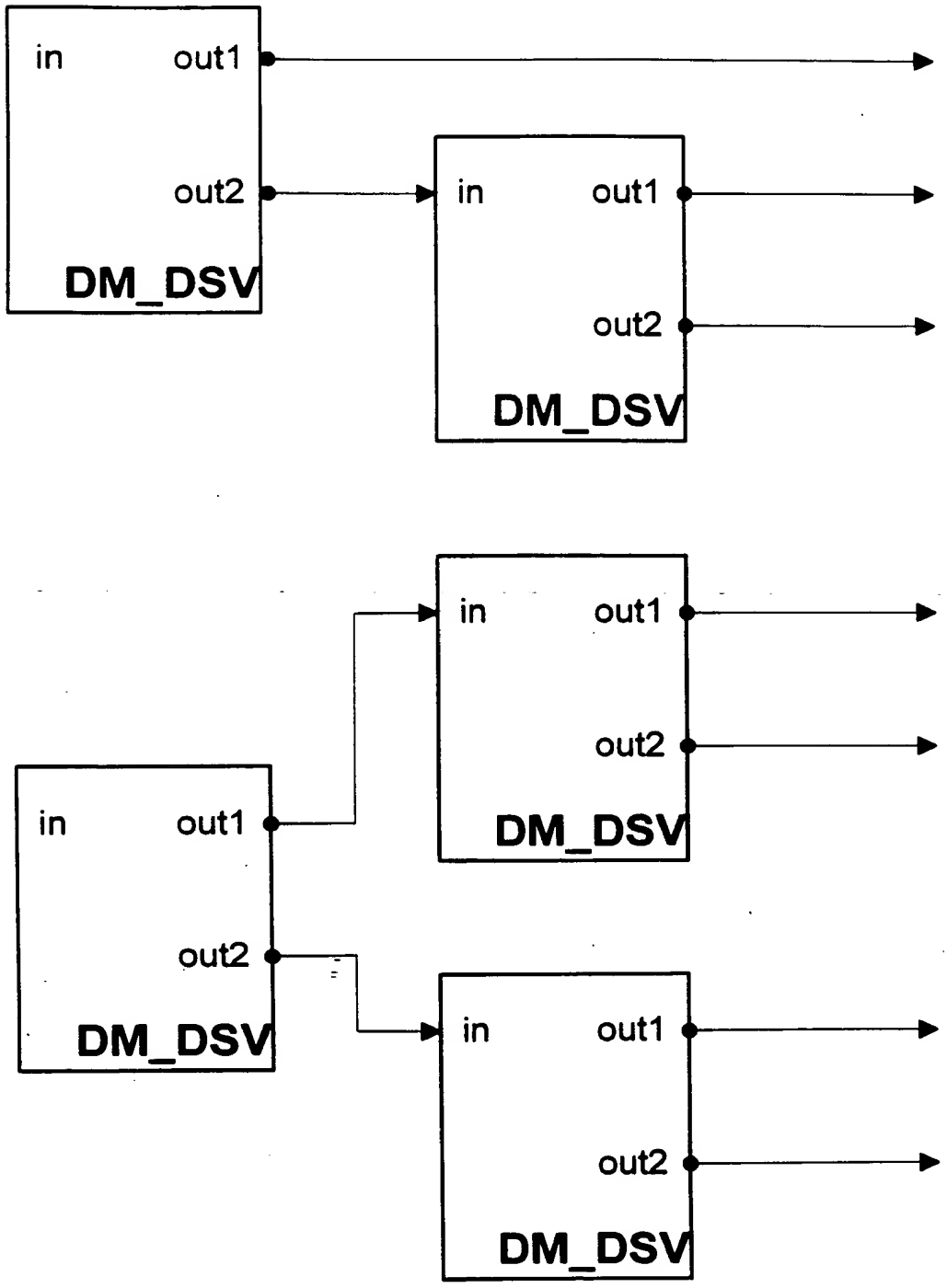


Fig. 36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out1
out2
DM_DSV
in
out1
out2
DM_DSV
in
out1
out2
DM_DSV
in
out1
out2
DM_DSV
in
out1
out2
DM_DSV

Fig. 37

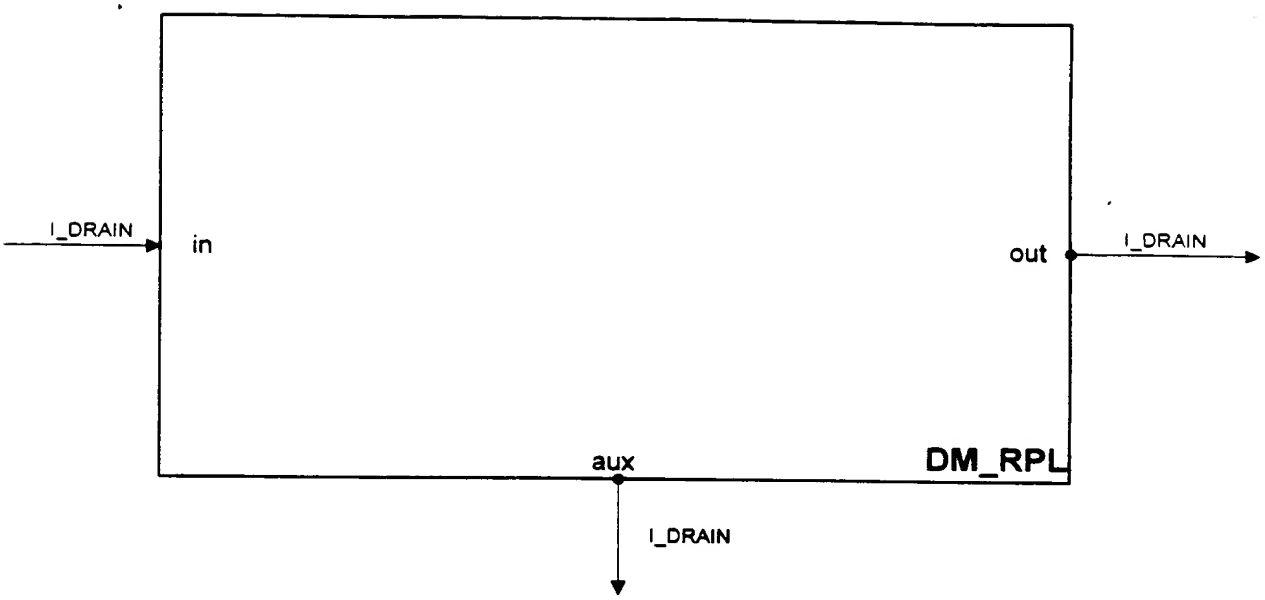


Fig. 38

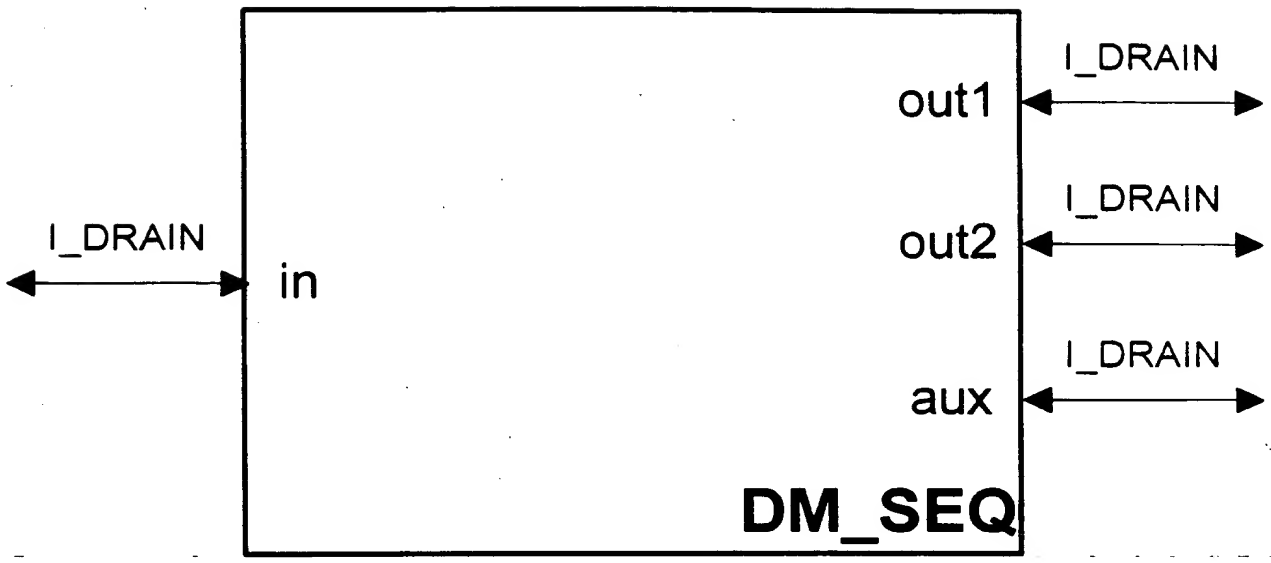


Fig. 39

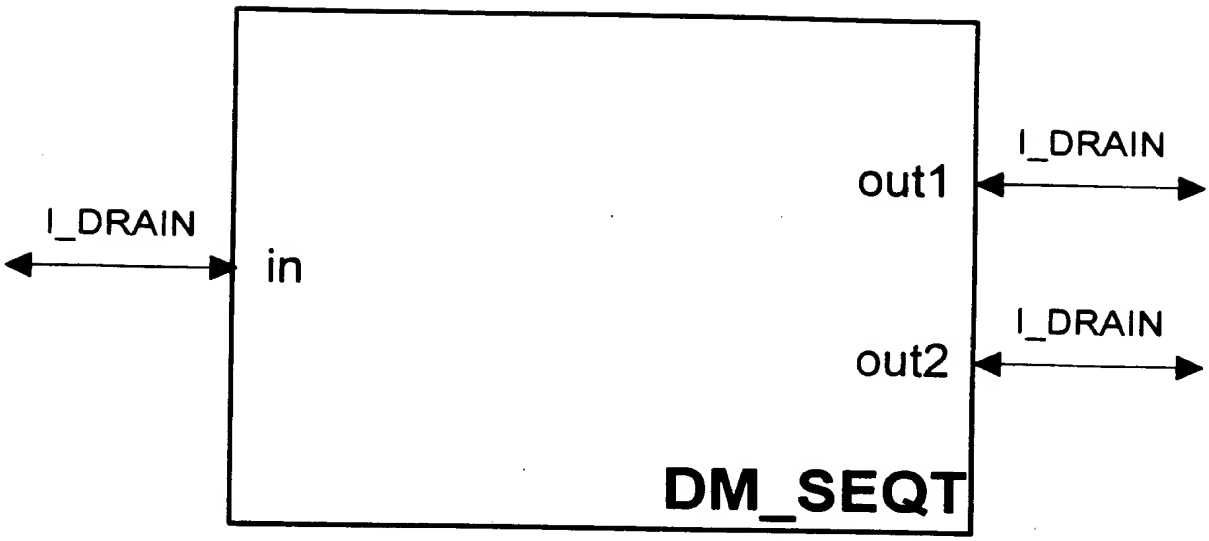
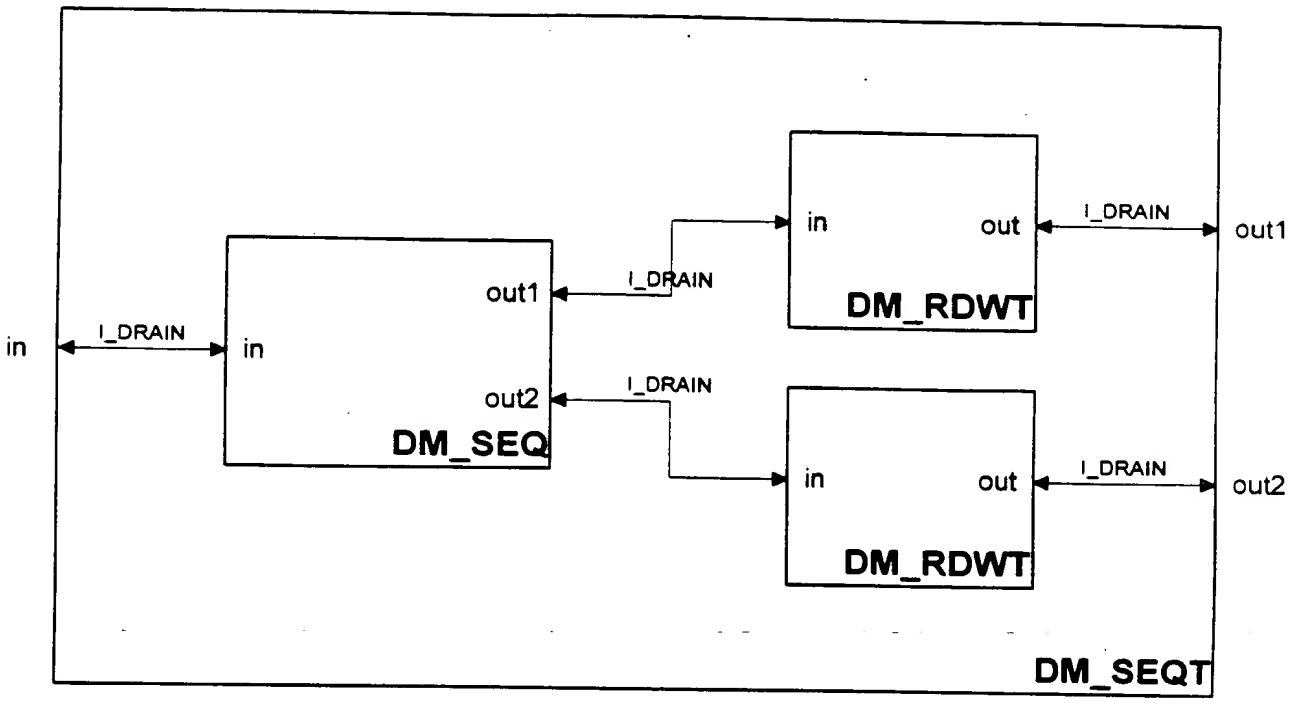


Fig. 40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out1
out2
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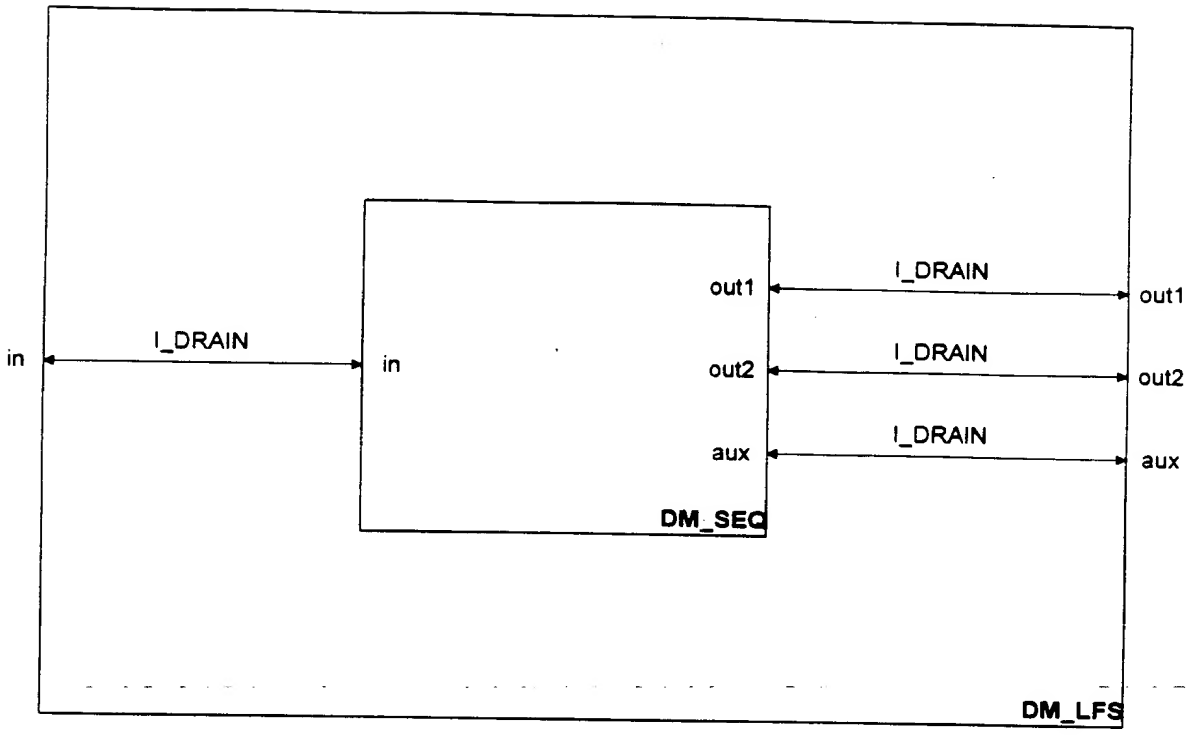
I_DRAIN
I_DRAIN
in
out
DM_RDWT
I_DRAIN
out1
in
out
DM_RDWT
I_DRAIN
out2
DM_SEQT

Fig. 41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I_DRAIN
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out1
out2
aux
DM_LFS

Fig. 42

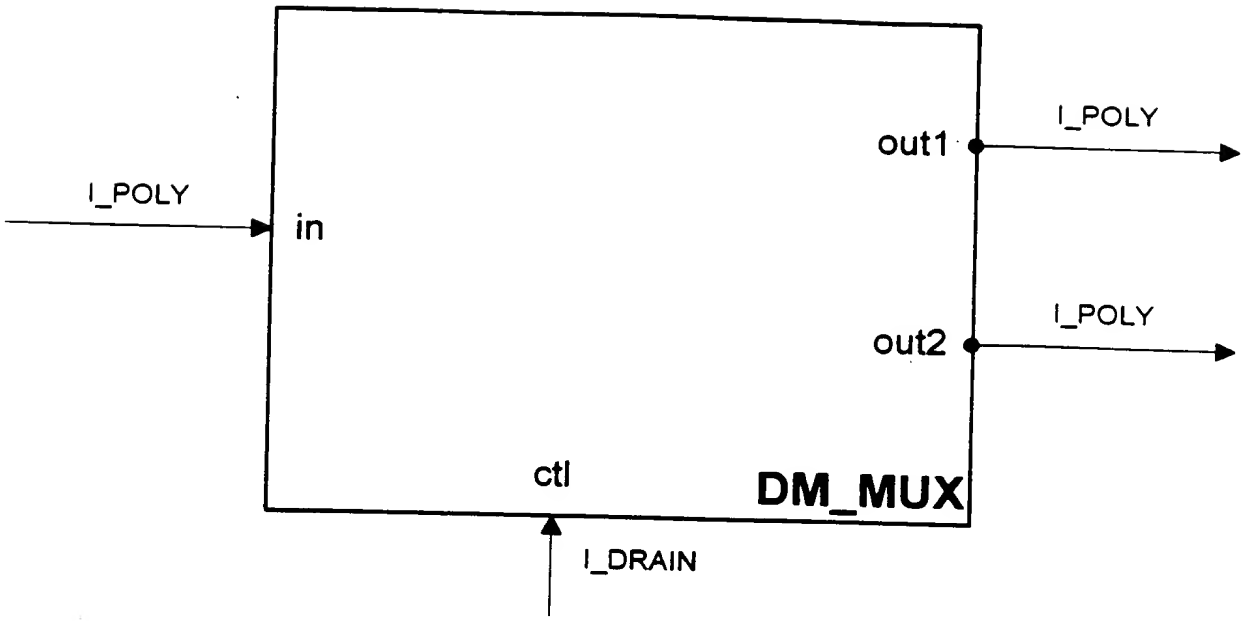


Fig. 43

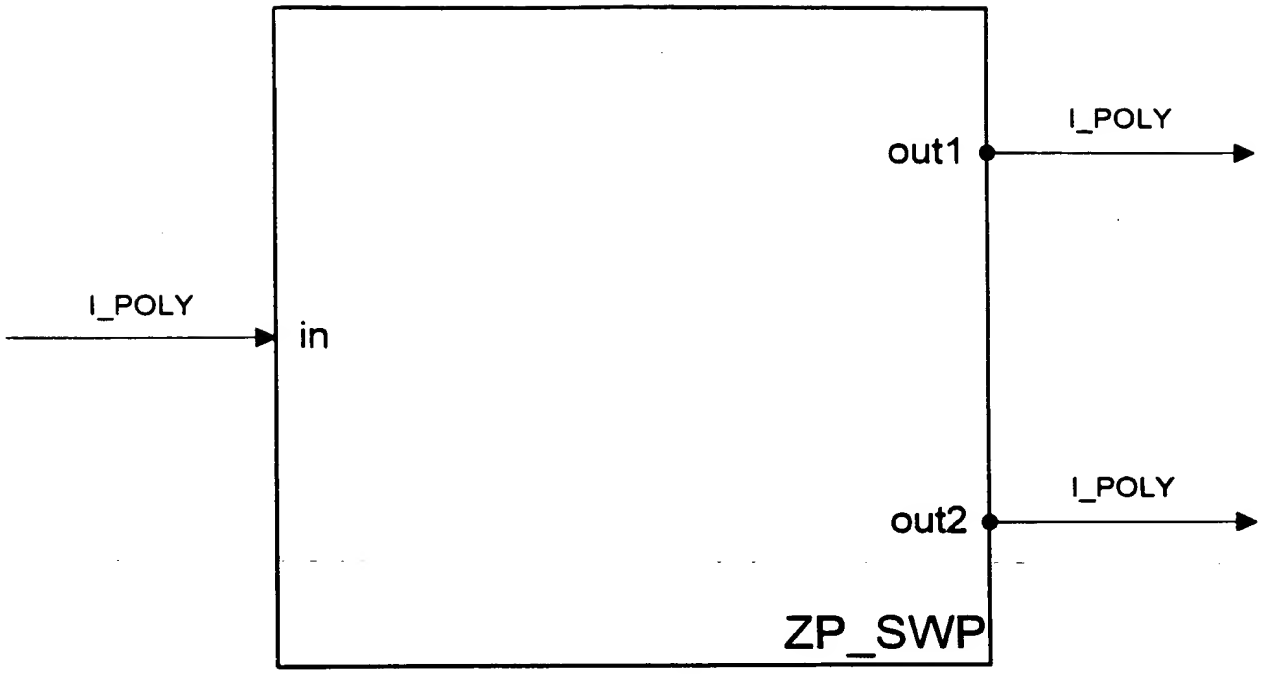


Fig. 44

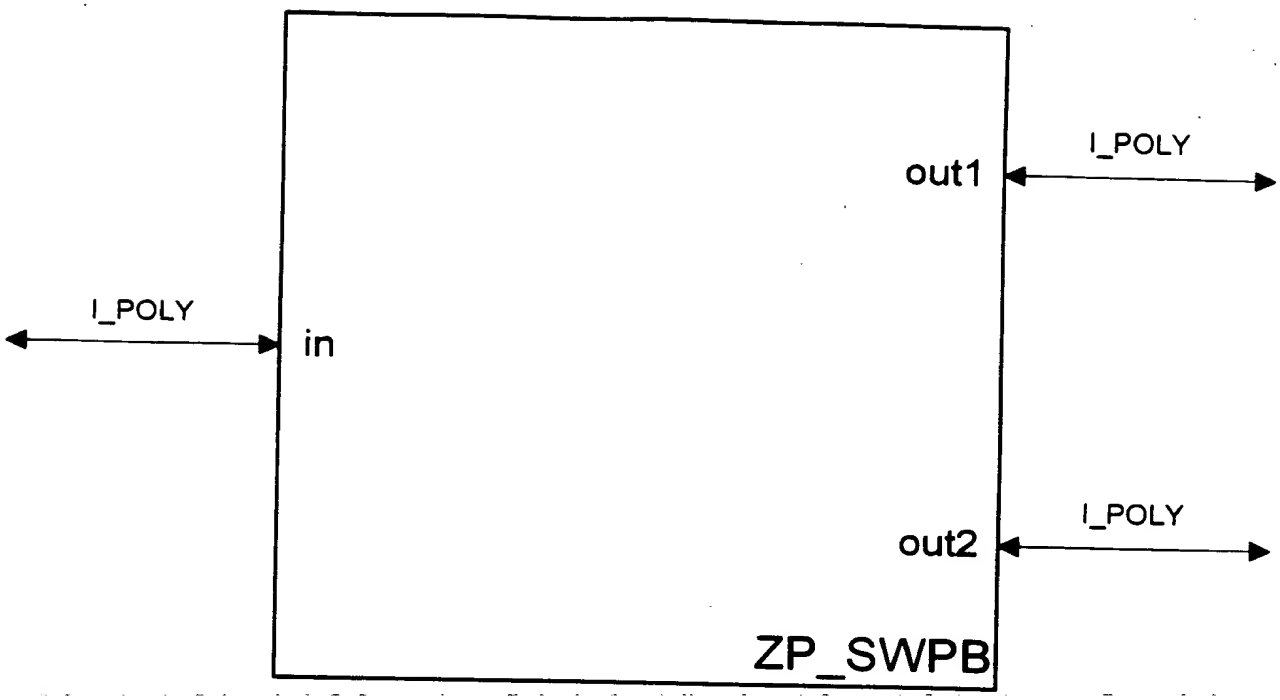


Fig. 45

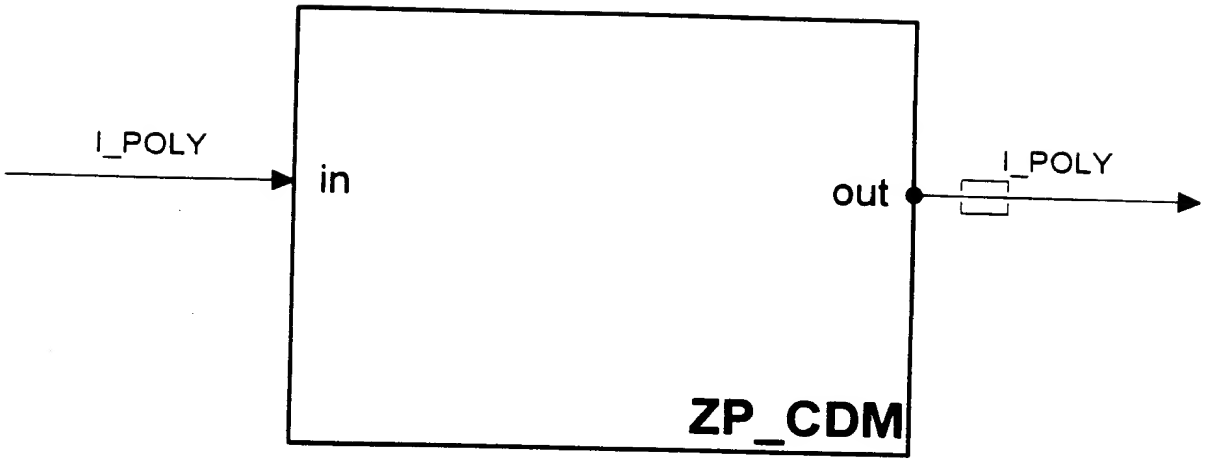


Fig. 46

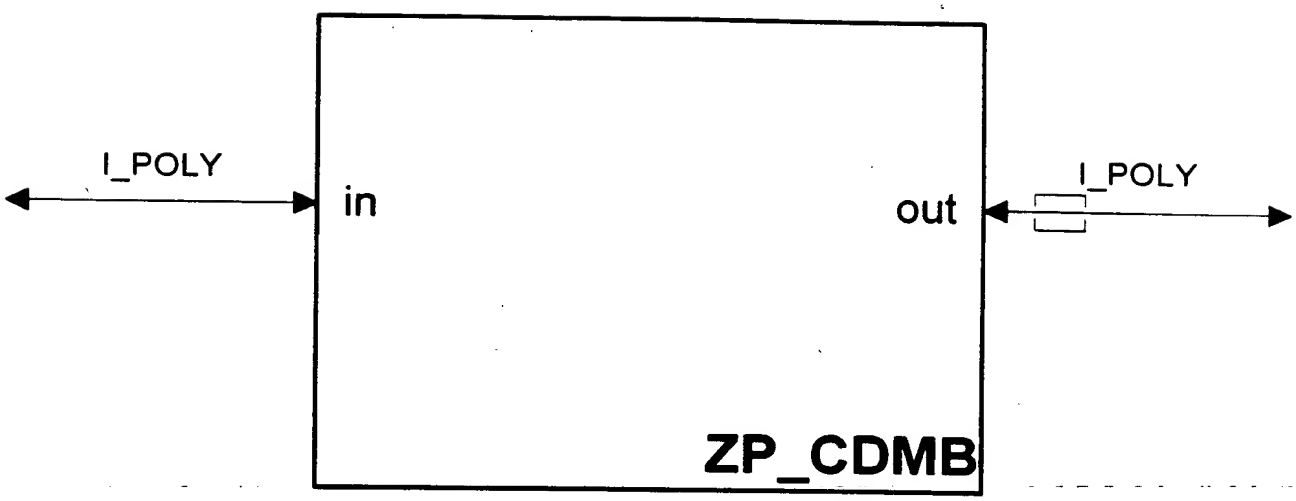


Fig. 47

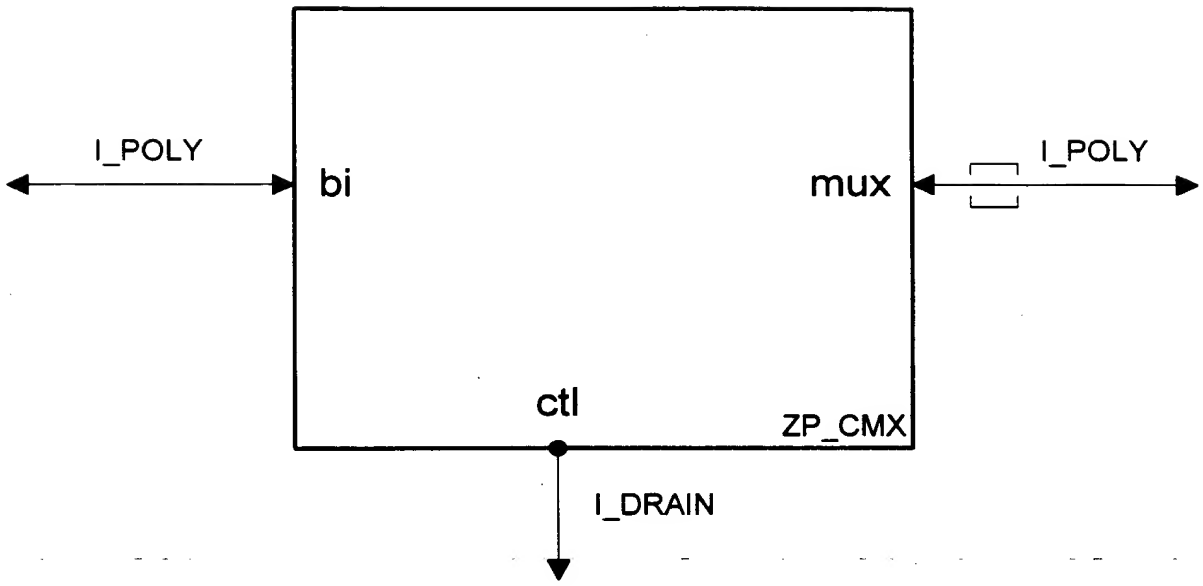


Fig. 48

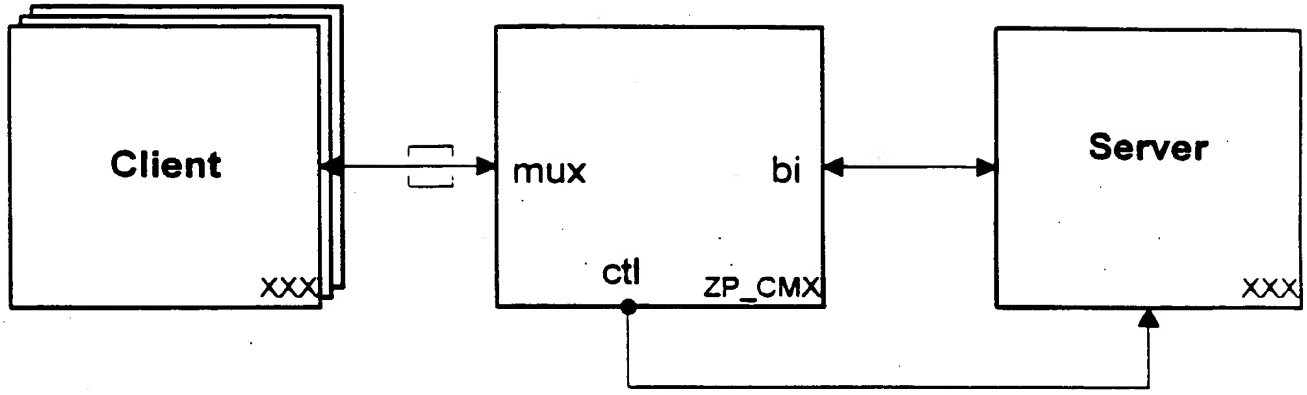
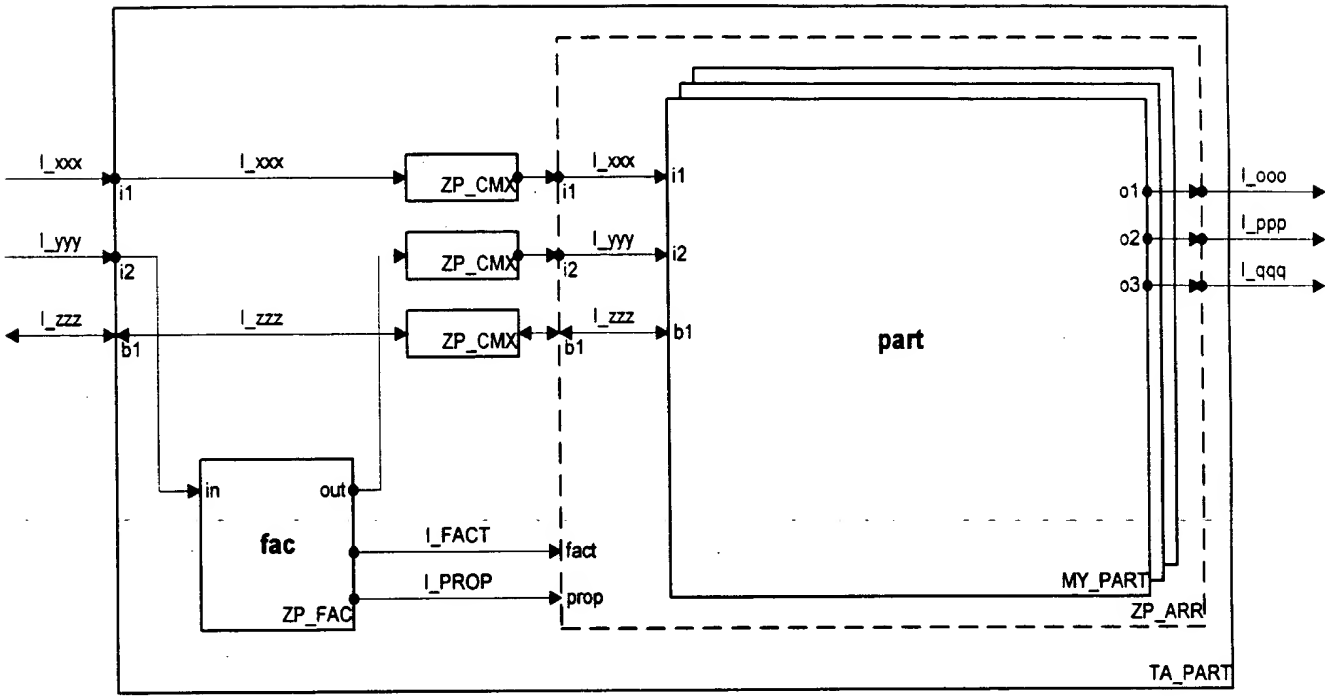


Fig. 49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i1
I_yyy
i2
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b1
I_zzz
ZP_CMX
I_zzz
b1
in
out
fac
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fact
I_PROP
prop
ZP_FAC
part
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o2
o3
I_ooo
I_ppp
I_qqq
MY_PART
ZP_ARR
TA_PART

Fig. 50

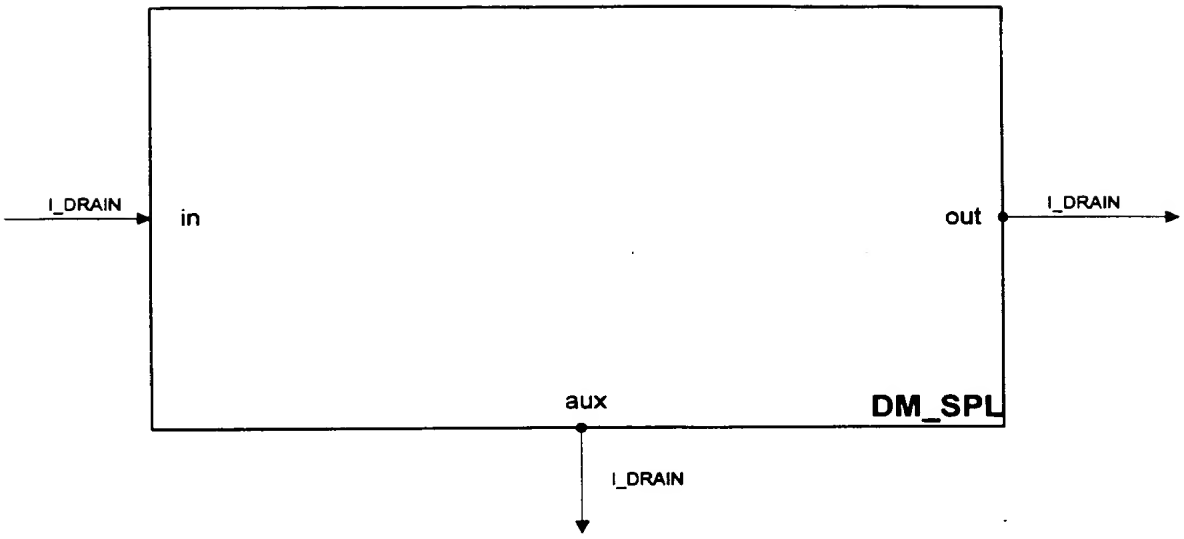


Fig. 51

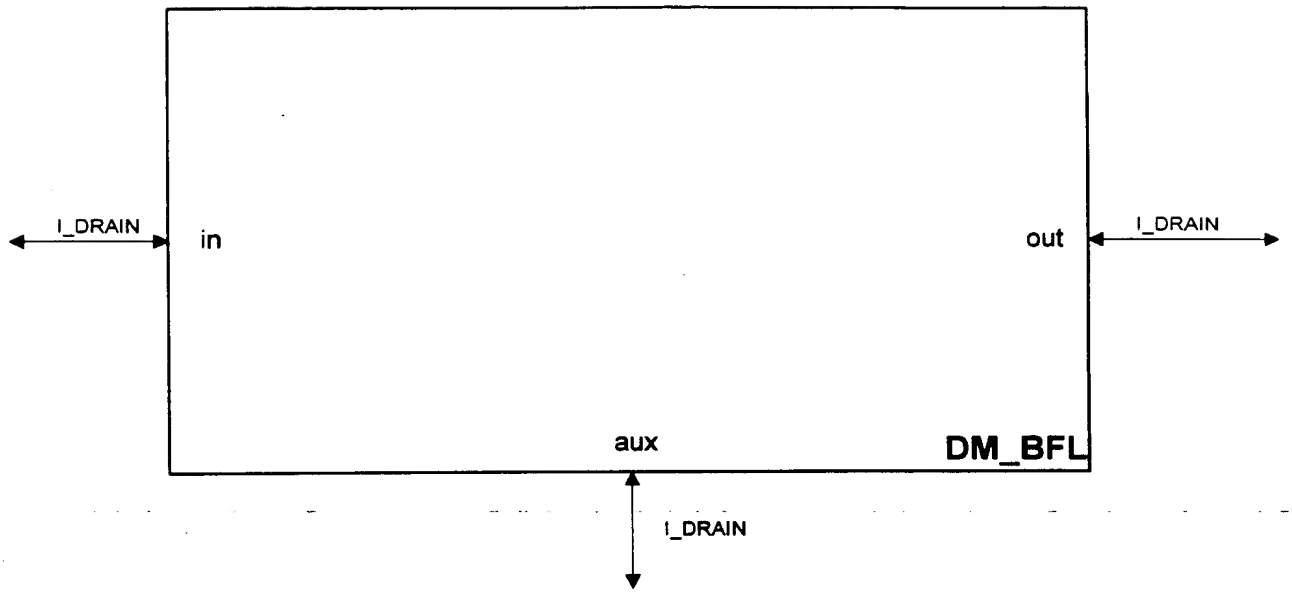
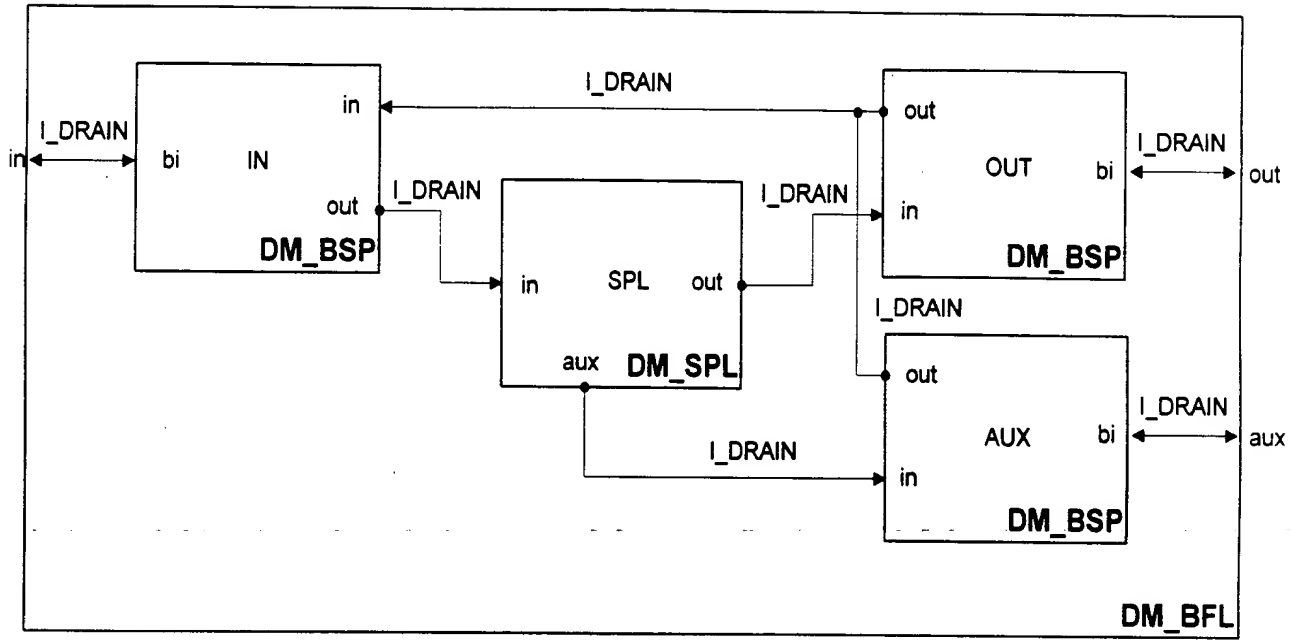


Fig. 52


I_DRAIN
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DM_BSP
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in
SPL
out
aux
DM_SPL
I_DRAIN
out
OUT
bi
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I_DRAIN
out
AUX
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in
DM_BSP
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aux
DM_BFL

Fig. 53

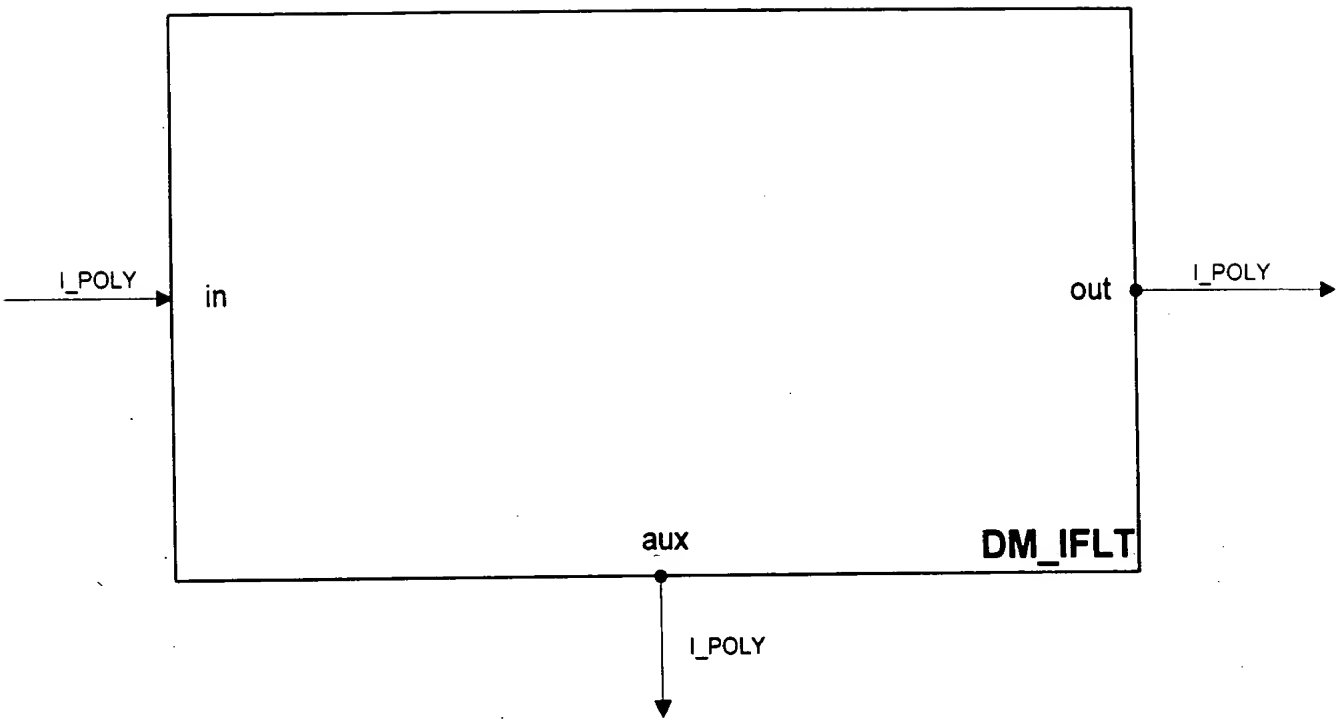


Fig. 54

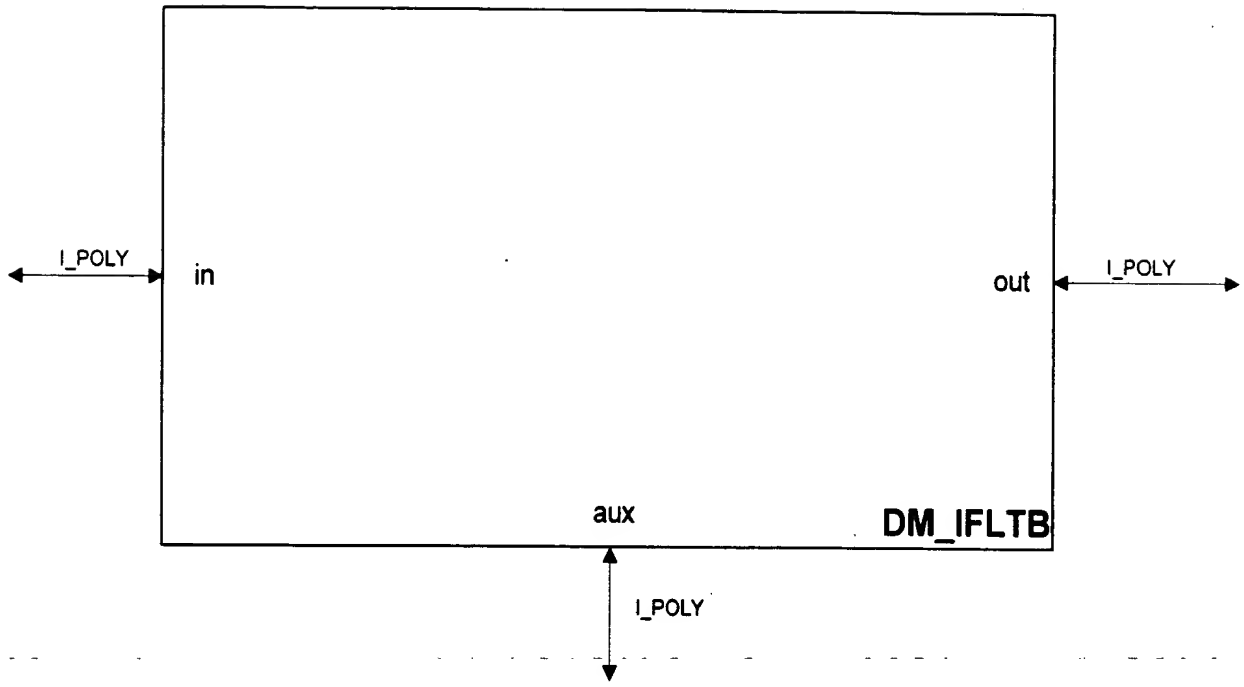


Fig. 55

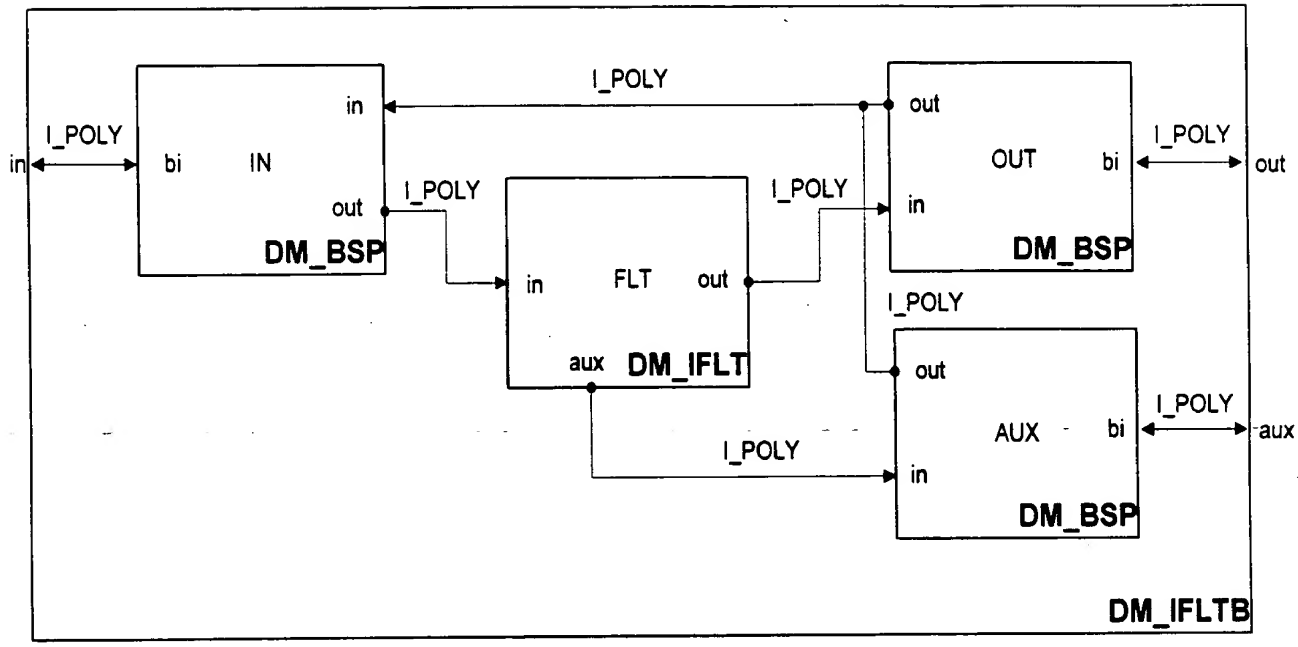

I_POLY
in
I_POLY
bi
IN
in
out
DM_BSP
I_POLY
I_POLY
in
FLT
out
aux
DM_IFLT
I_POLY
out
OUT
bi
in
DM_BSP
I_POLY
out
I_POLY
out
AUX
bi
I_POLY
in
DM_BSP
DM_IFLTB

Fig. 56

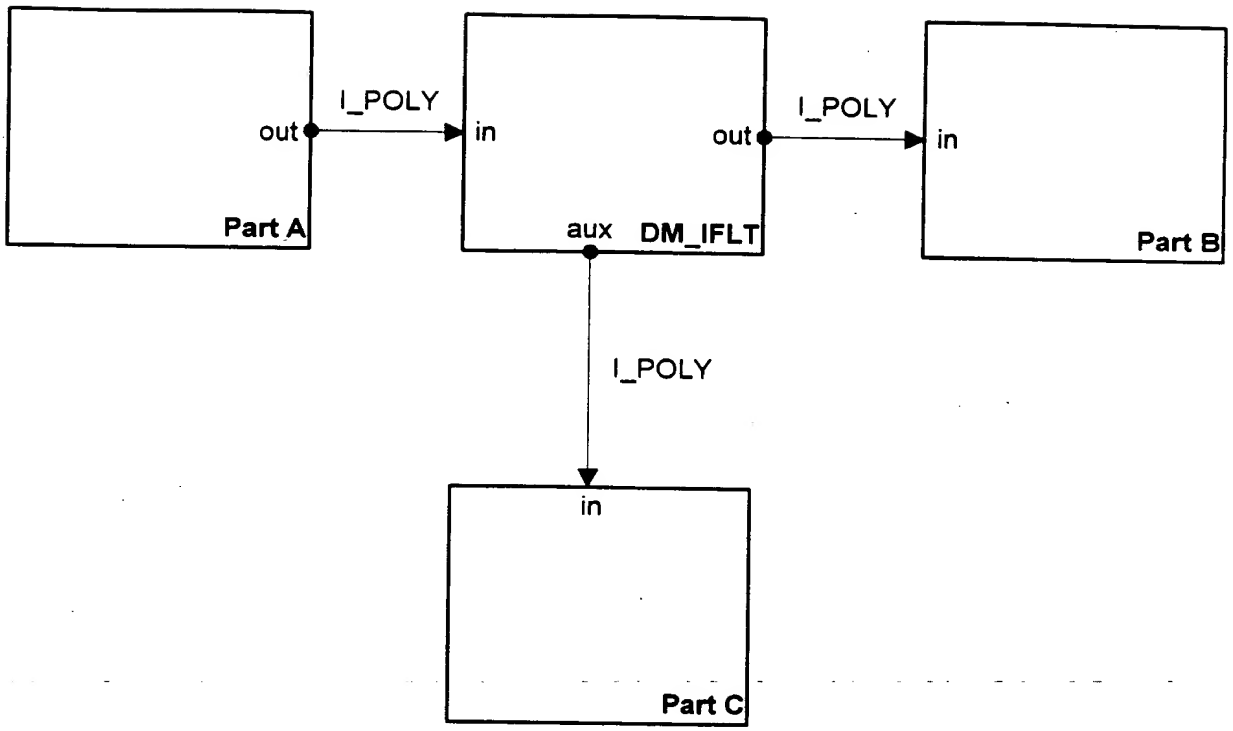

out
I_POLY
in
out
I_POLY
in
Part A
aux
DM_IFLT
Part B
I_POLY
in
Part C

Fig. 57

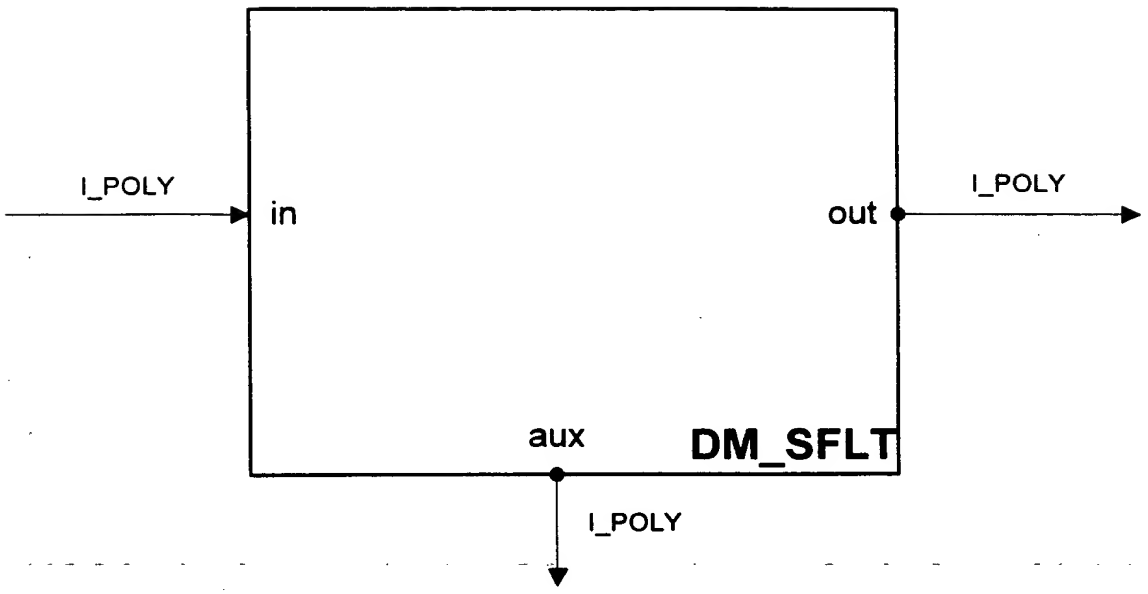


Fig. 58

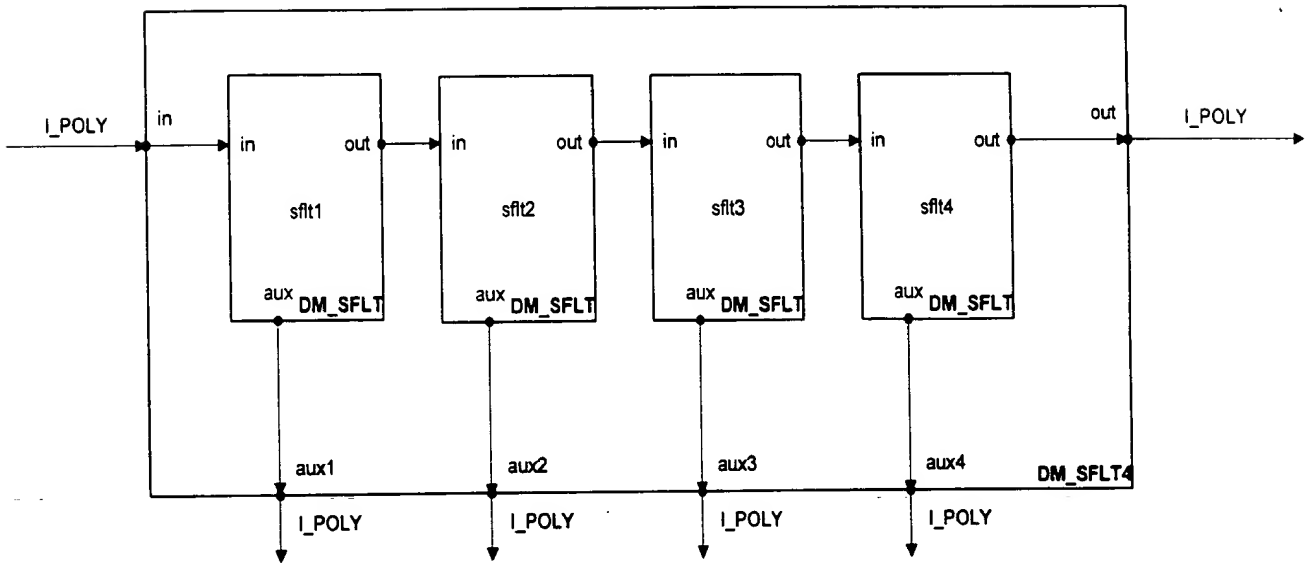

I_POLY
in
in
out
sflt1
aux
DM_SFLT
in
out
sflt2
aux
DM_SFLT
in
out
sflt3
aux
DM_SFLT
in
out
sflt4
aux
DM_SFLT
out
I_POLY
aux1
aux2
aux3
aux4
DM_SFLT4
I_POLY
I_POLY
I_POLY
I_POLY

Fig. 59

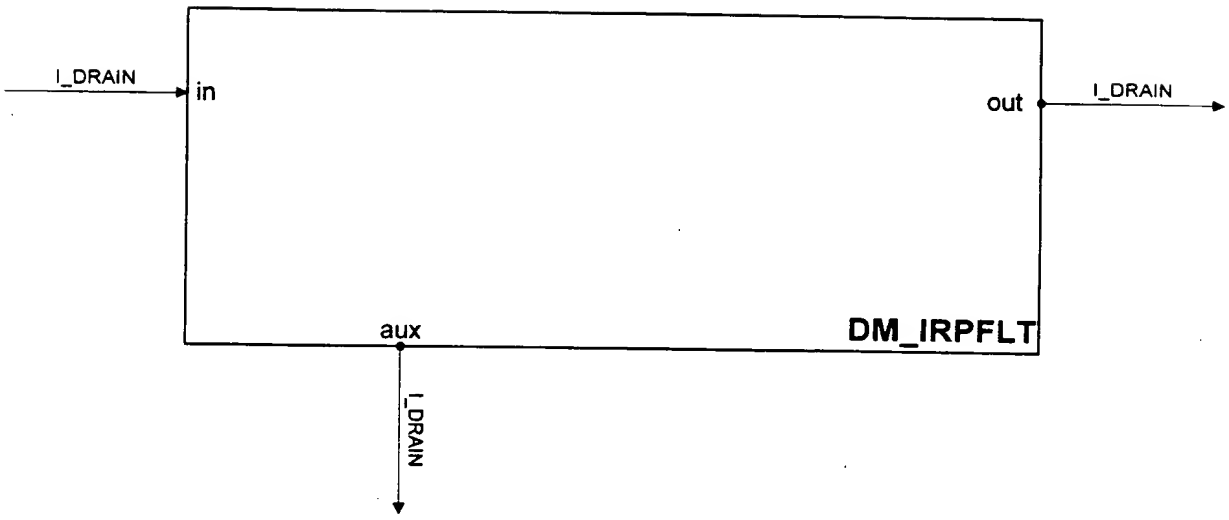


Fig. 60

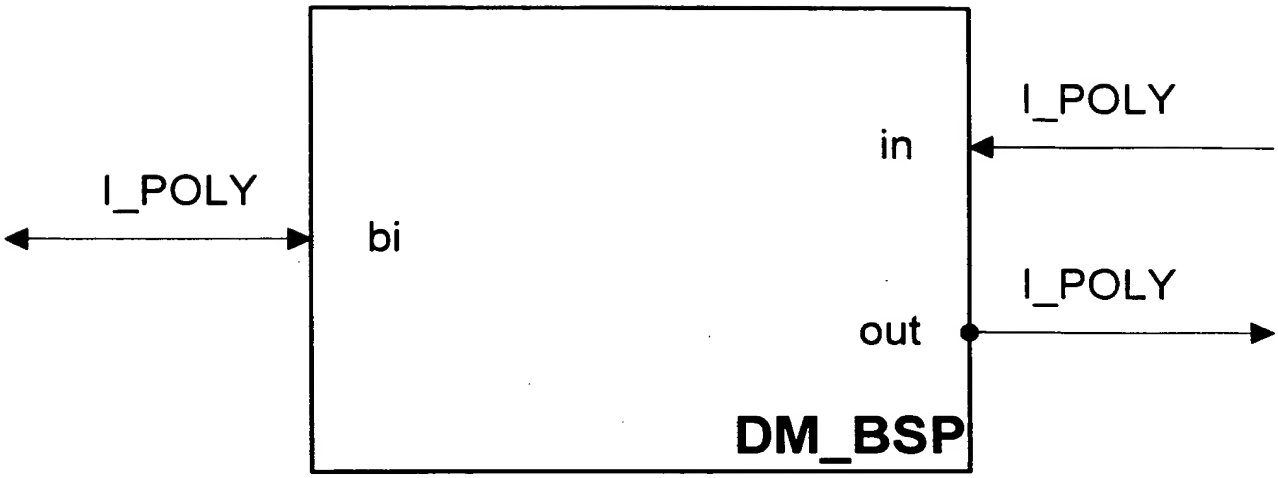


Fig. 61

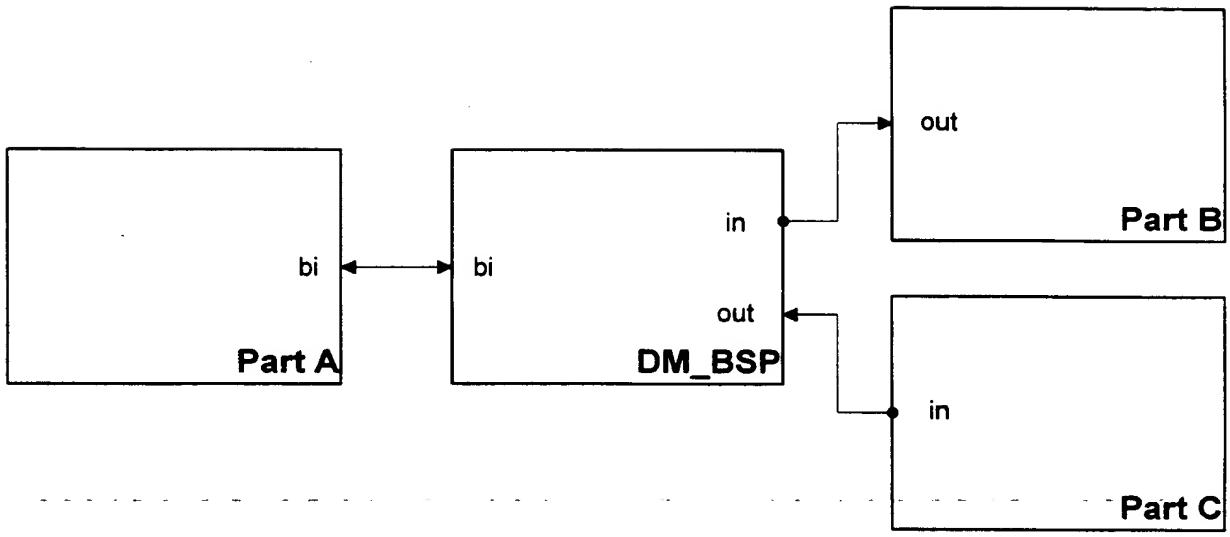


Fig. 62

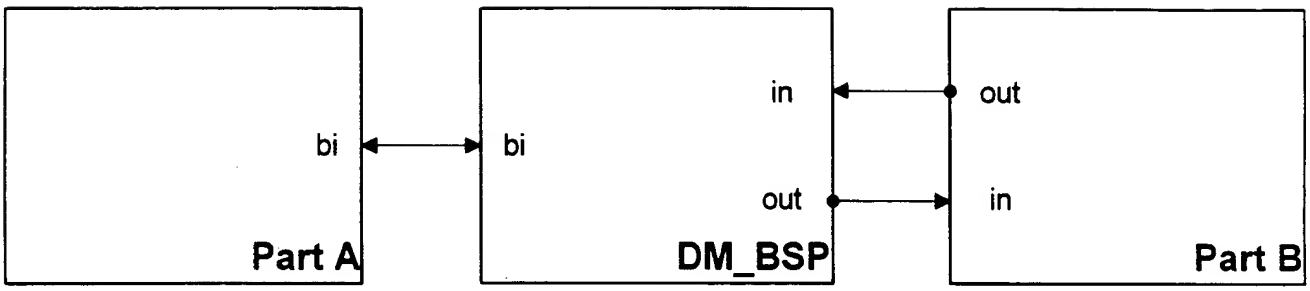


Fig. 63

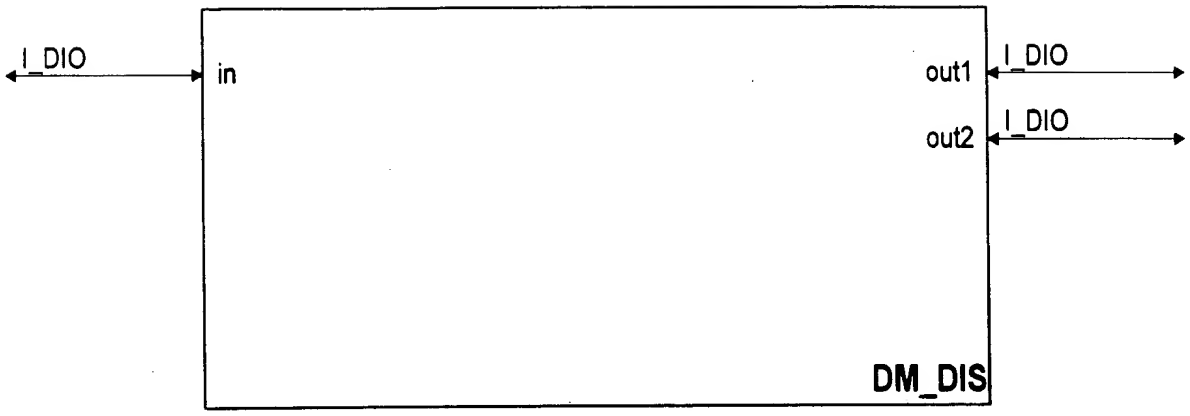


Fig. 64

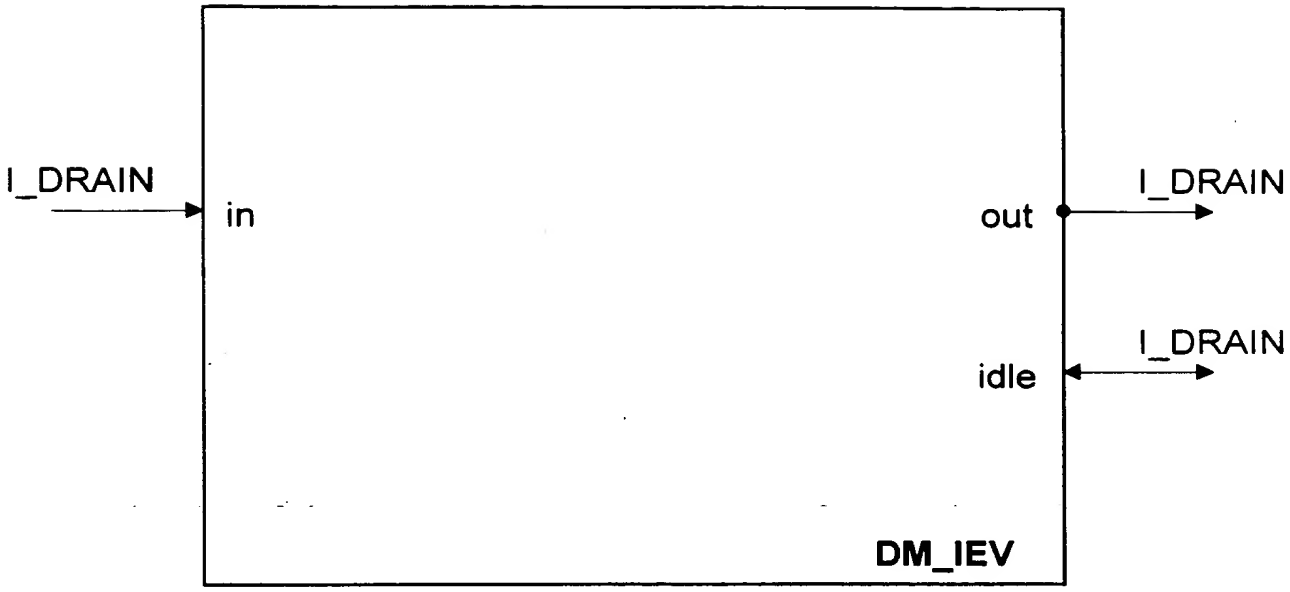


Fig. 65

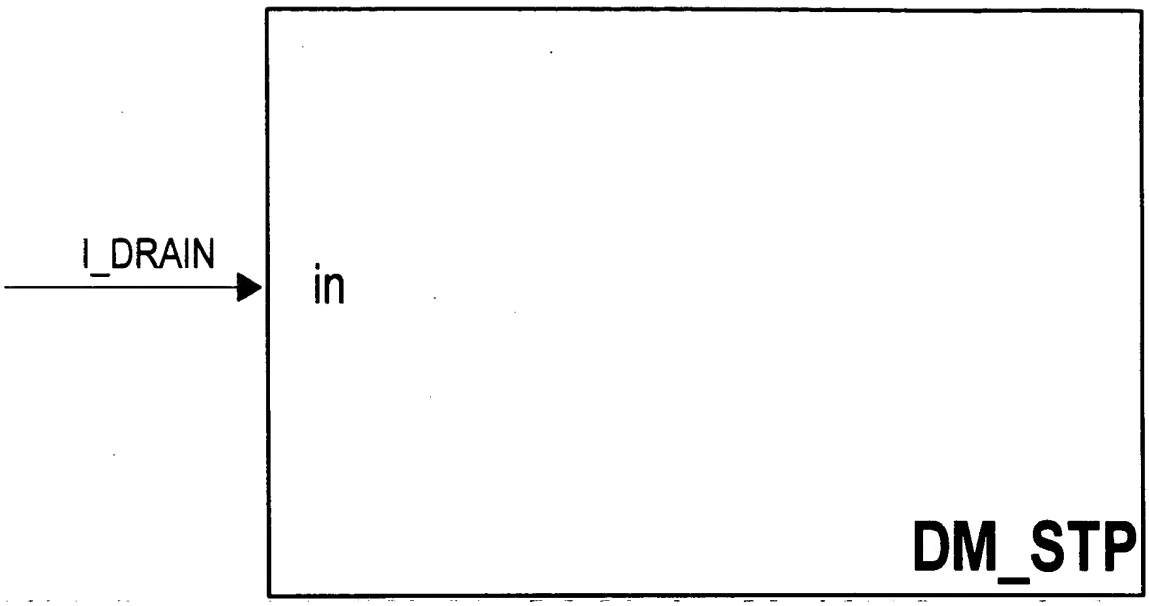


Fig. 66

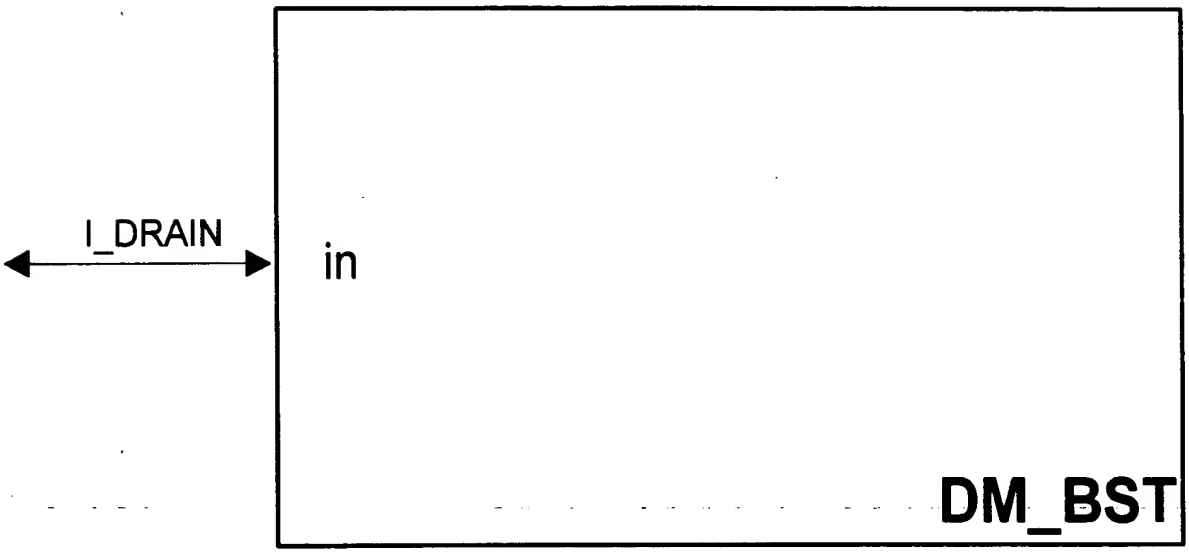


Fig. 67

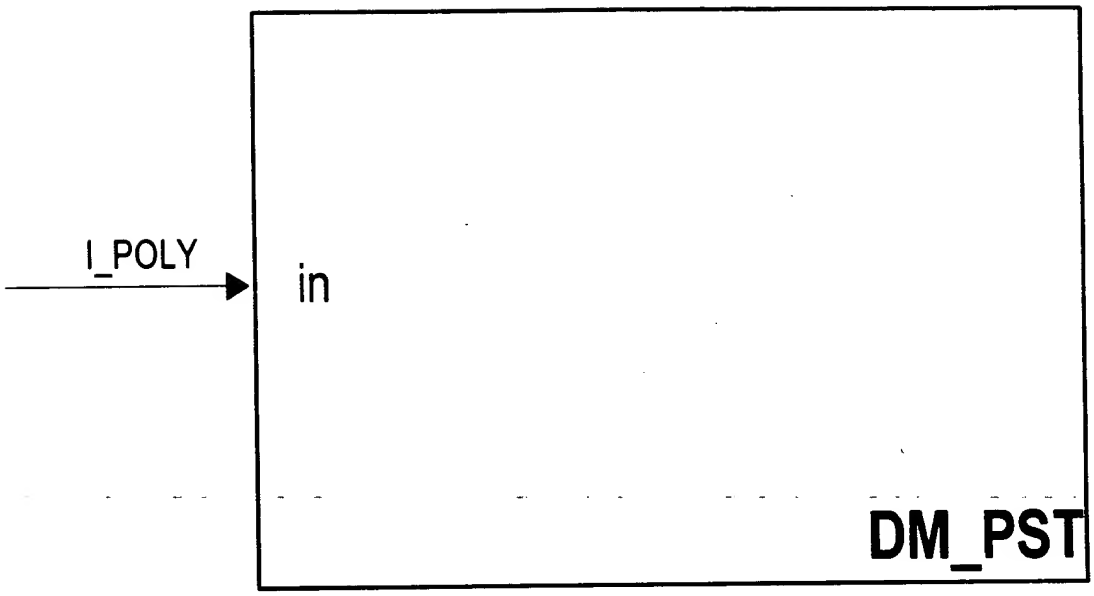


Fig. 68

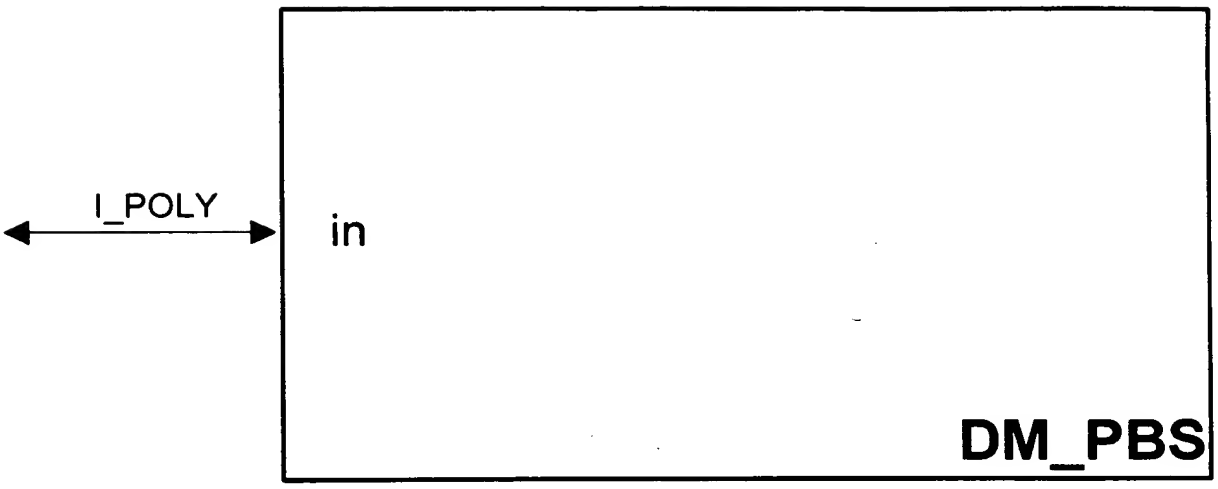


Fig. 69

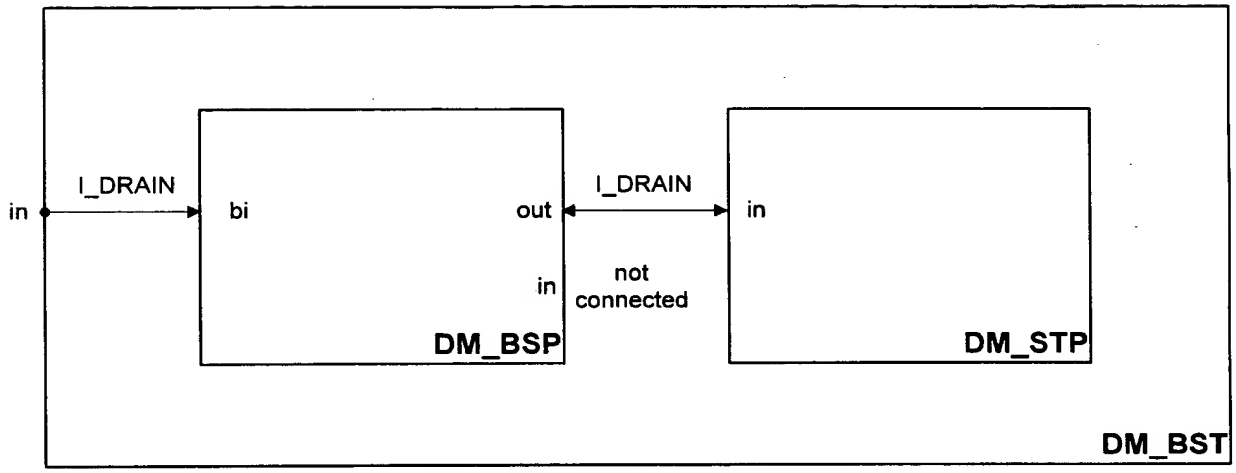

in
I_DRAIN
bi
out
in
DM_BSP
I_DRAIN
not
connected
in
DM_STP
DM_BST

Fig. 70

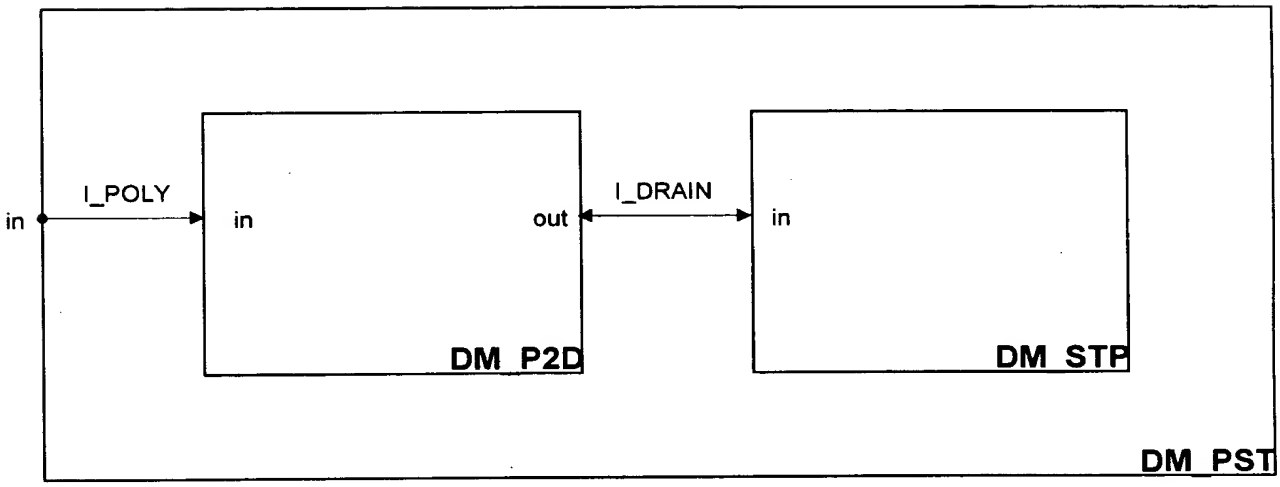


Fig. 71

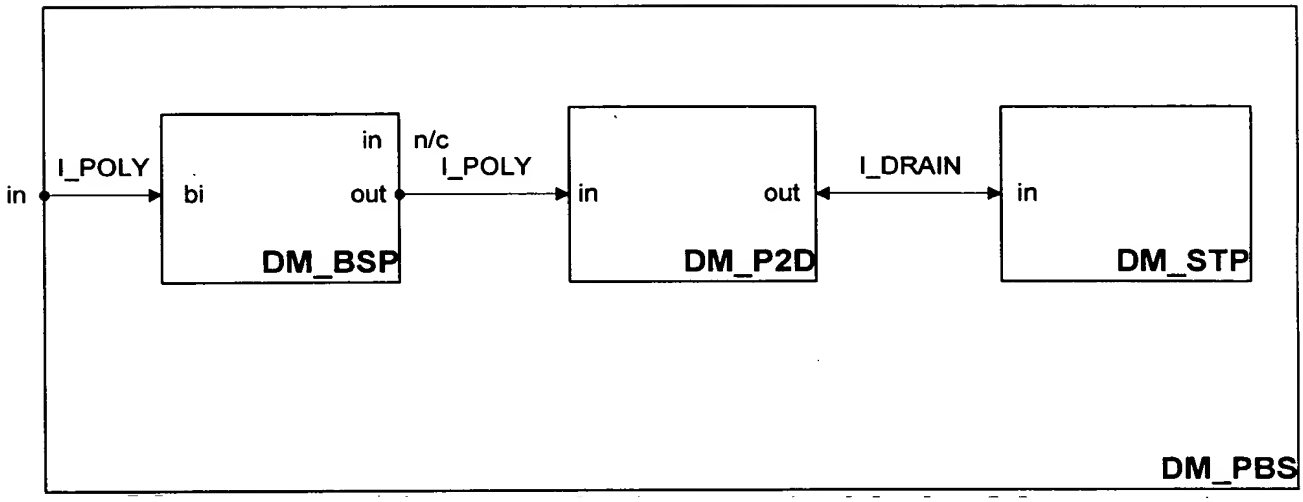

in
I_POLY
bi
in
out
n/c
I_POLY
DM_BSP
in
out
DM_P2D
I_DRAIN
in
DM_STP
DM_PBS

Fig. 72

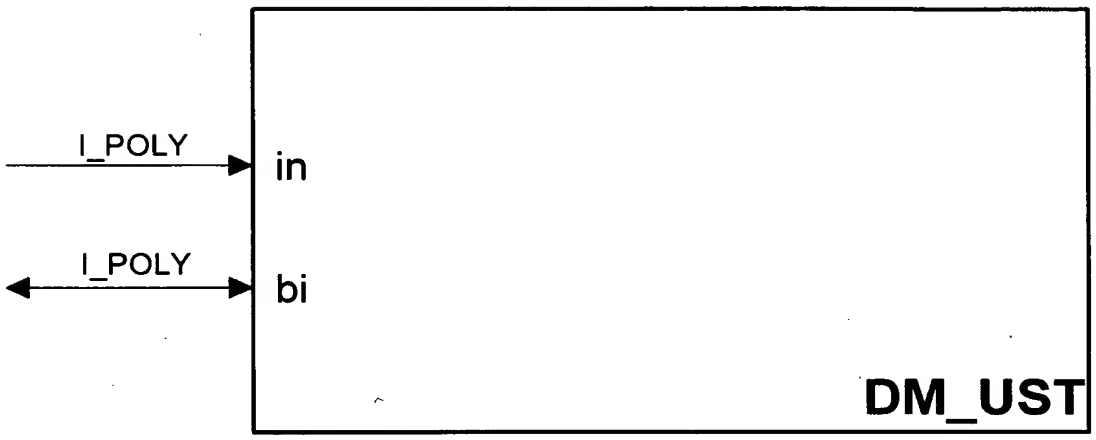


Fig. 73

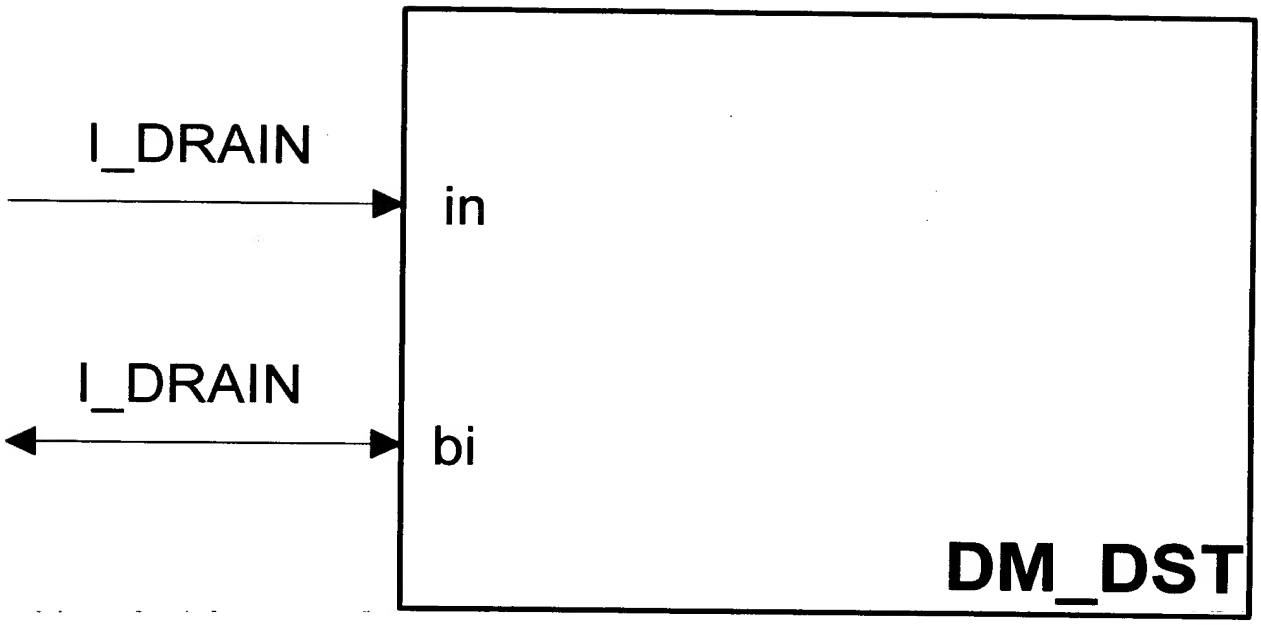


Fig. 74

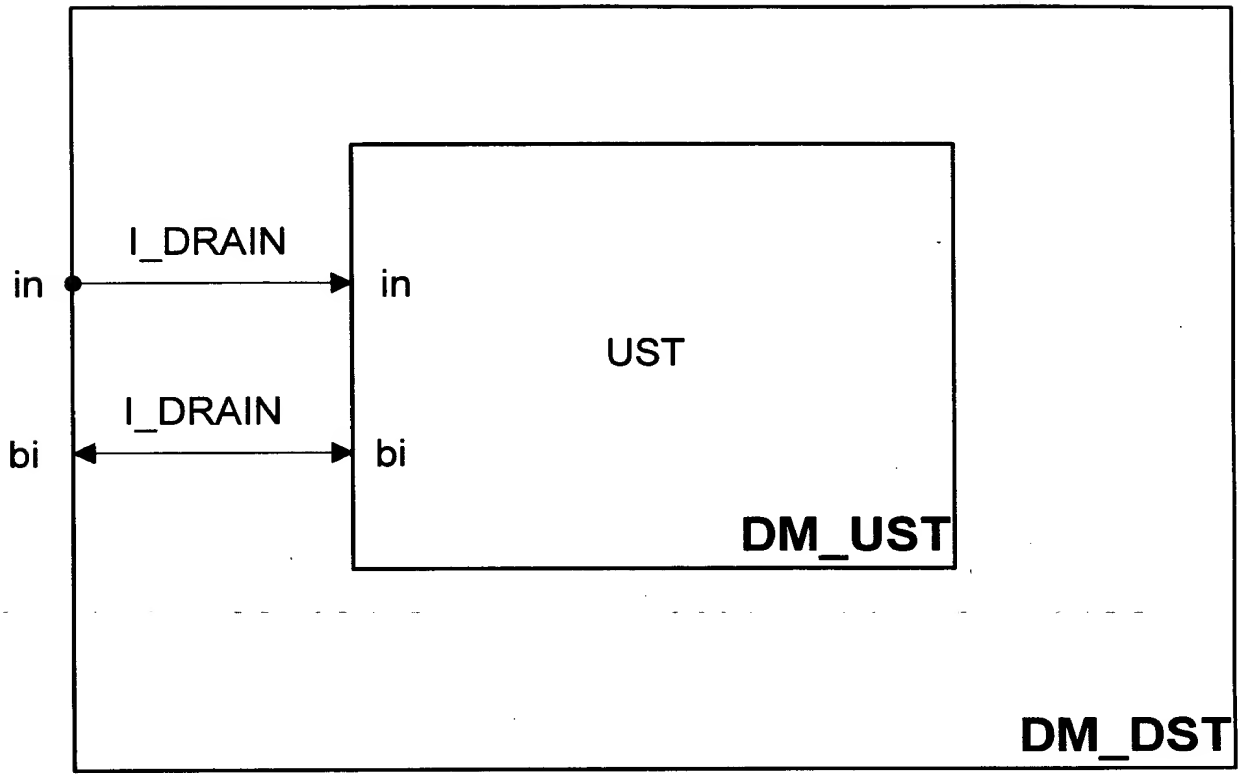


Fig. 75

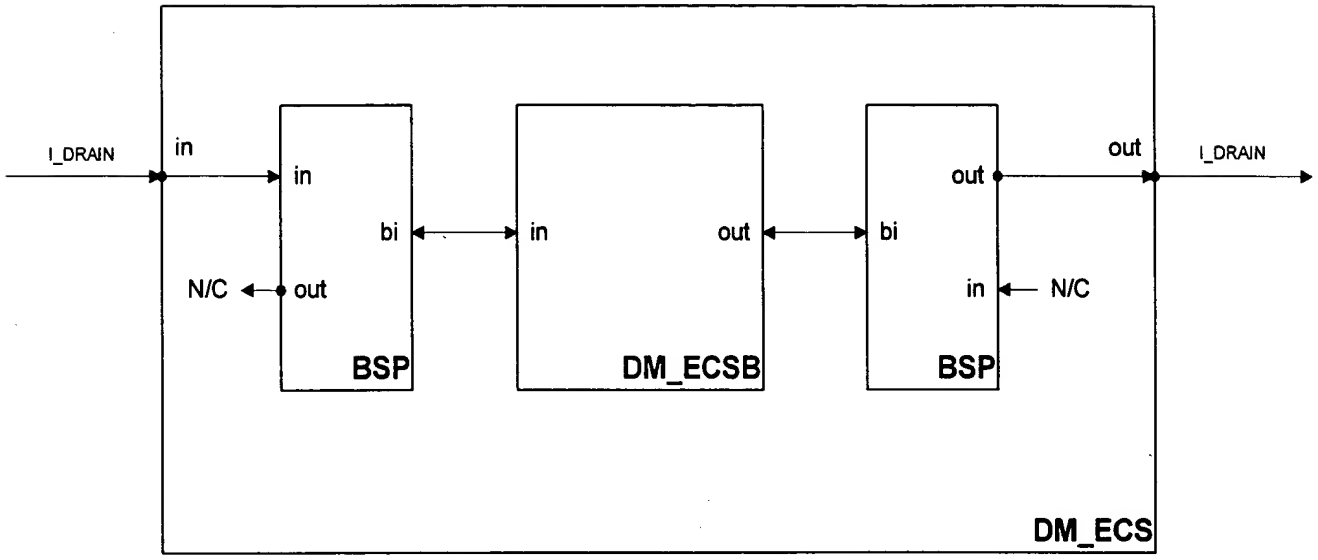

I_DRAIN
in
in
bi
N/C
out
BSP
in
out
DM_ECSB
bi
out
in
N/C
BSP
out
I_DRAIN
DM_ECS

Fig. 76

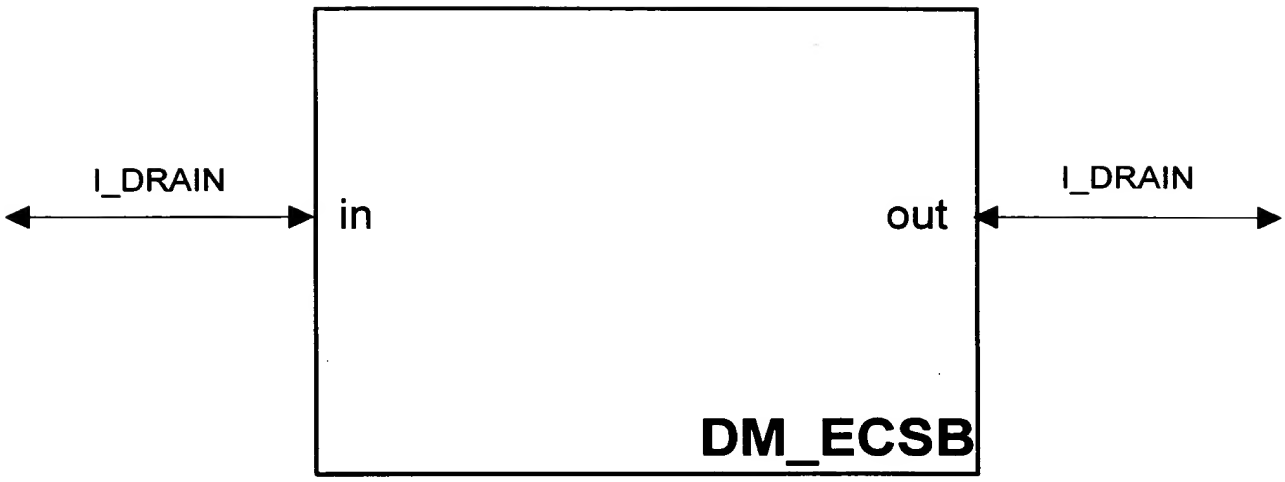


Fig. 77

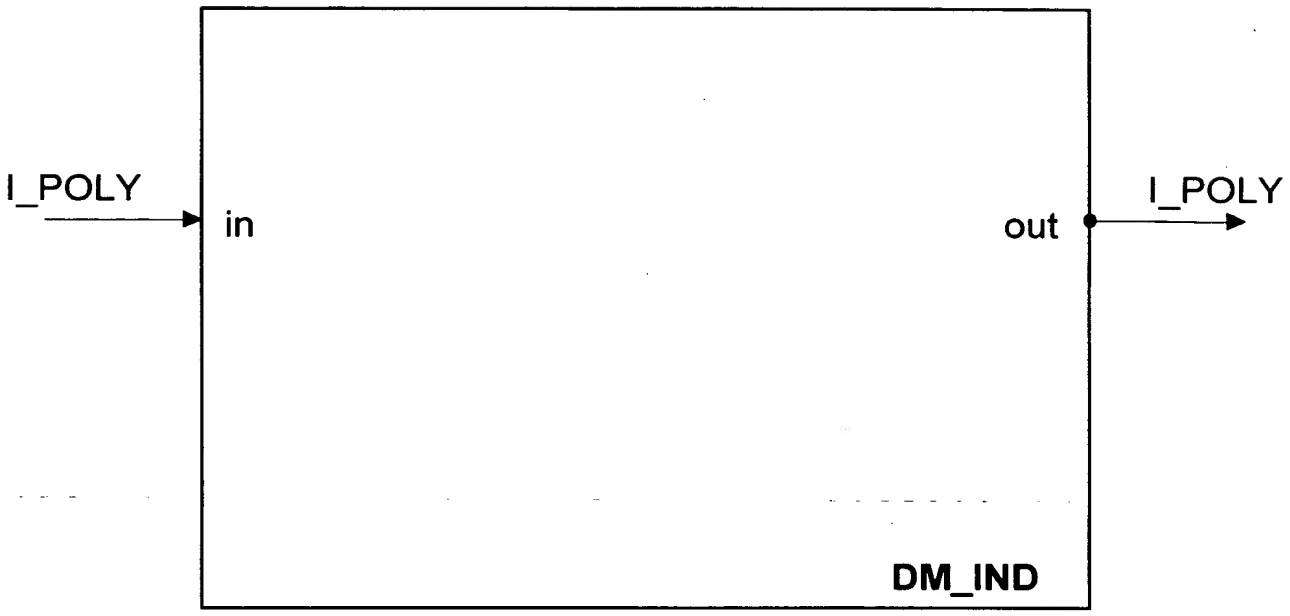


Fig. 78

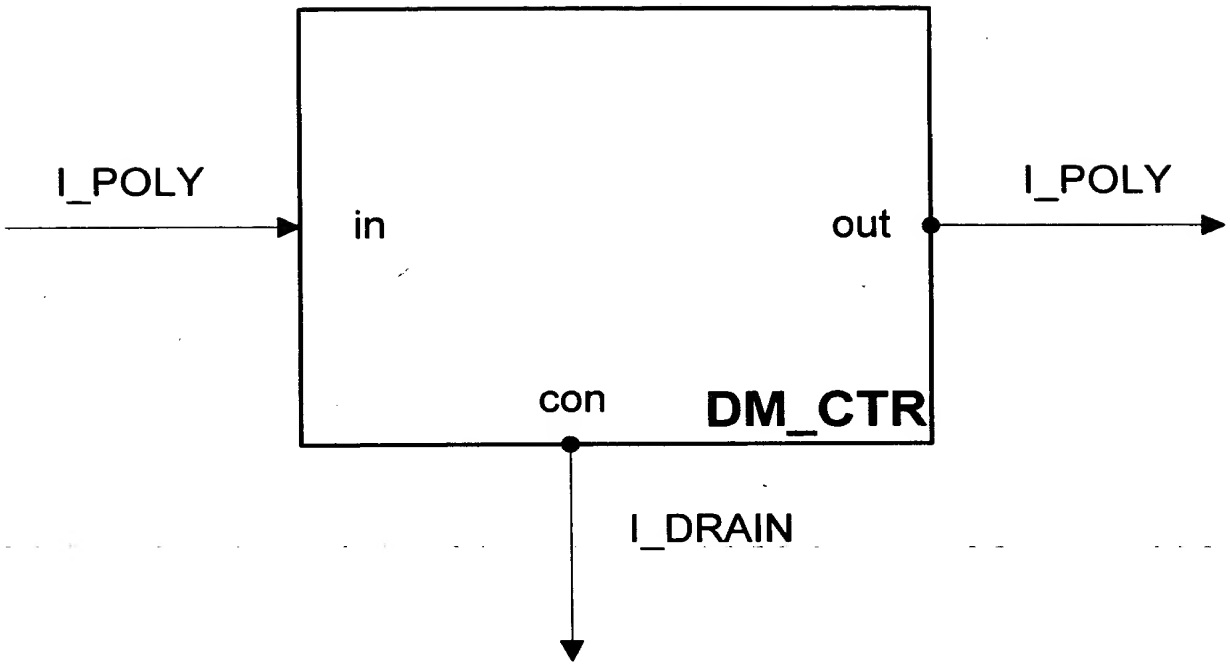


Fig. 79

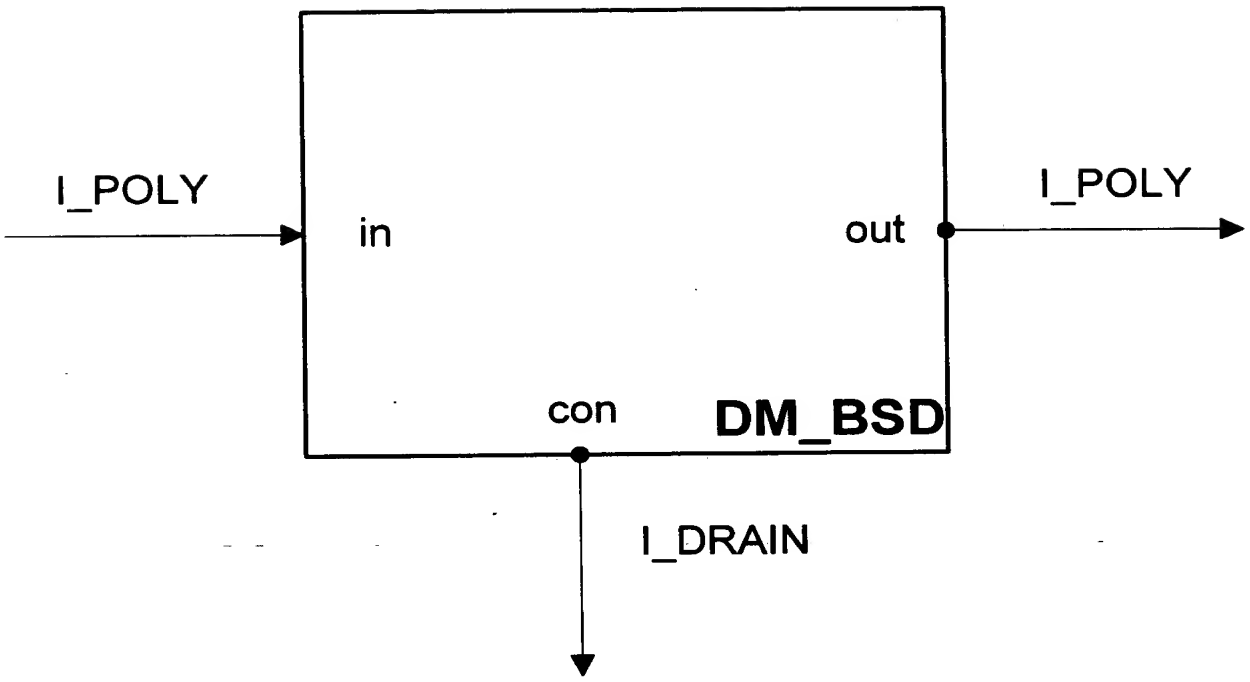


Fig. 80

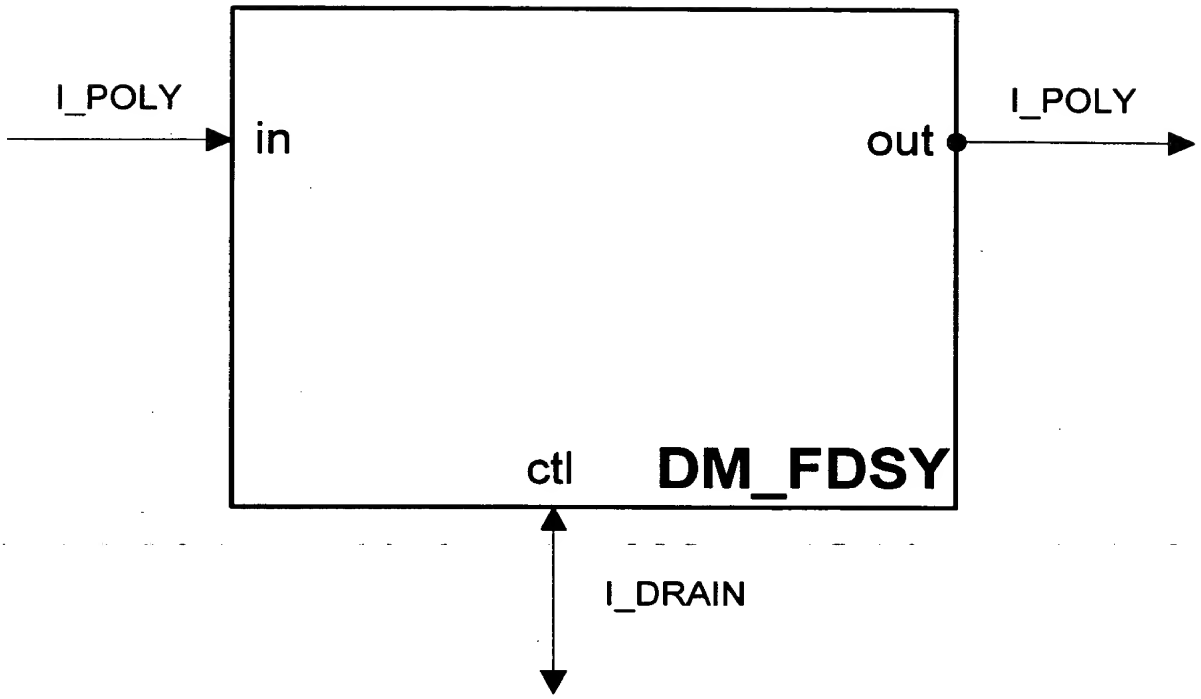


Fig. 81

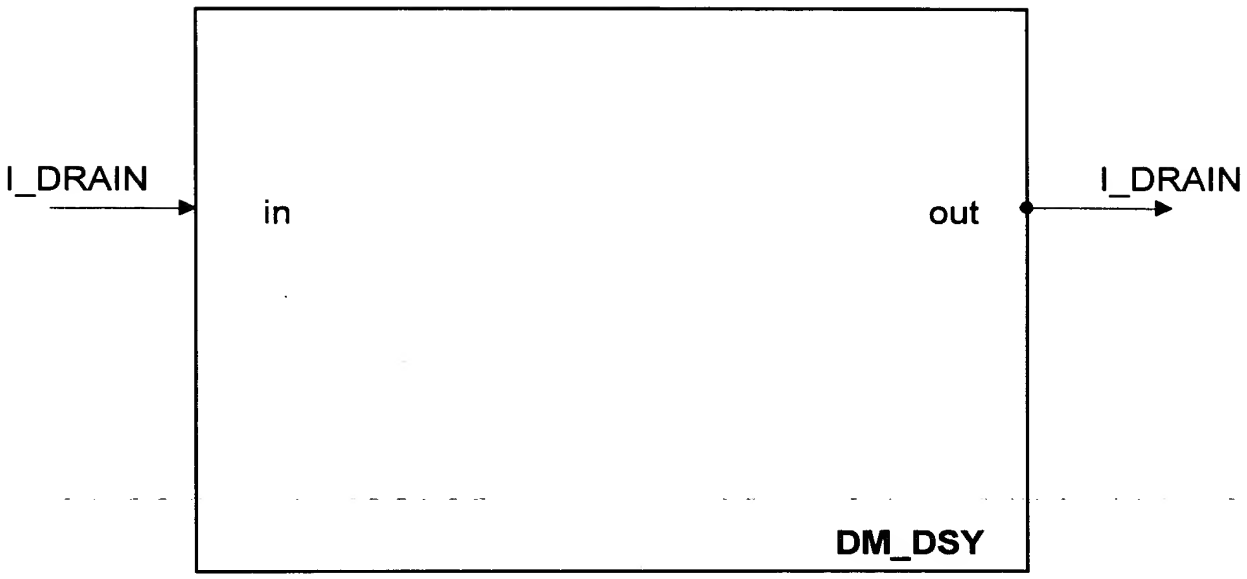


Fig. 82

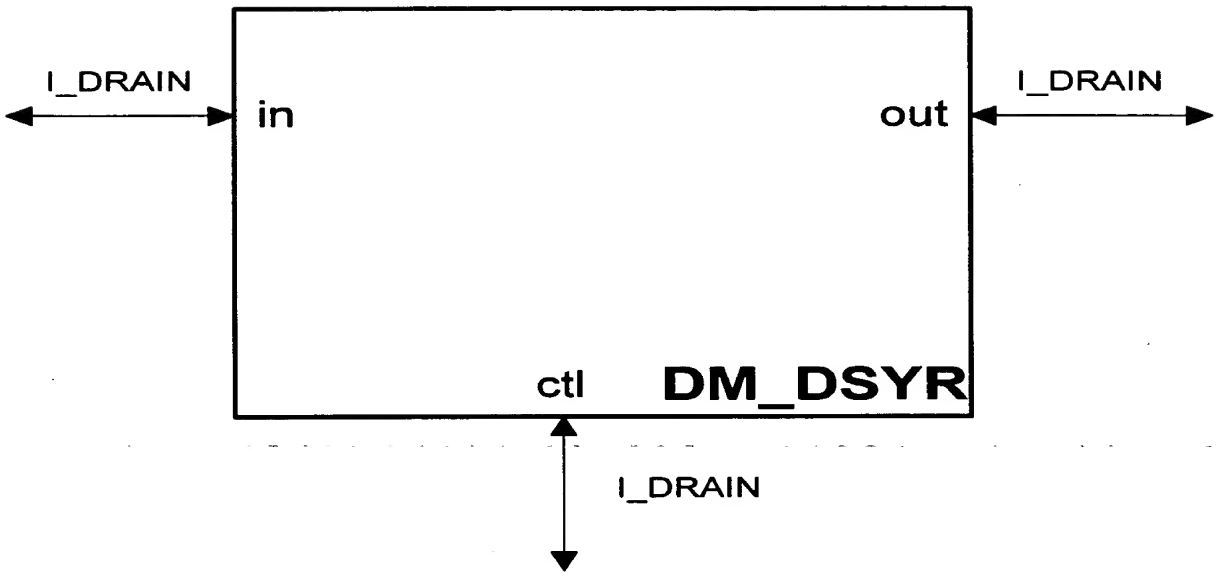


Fig. 83

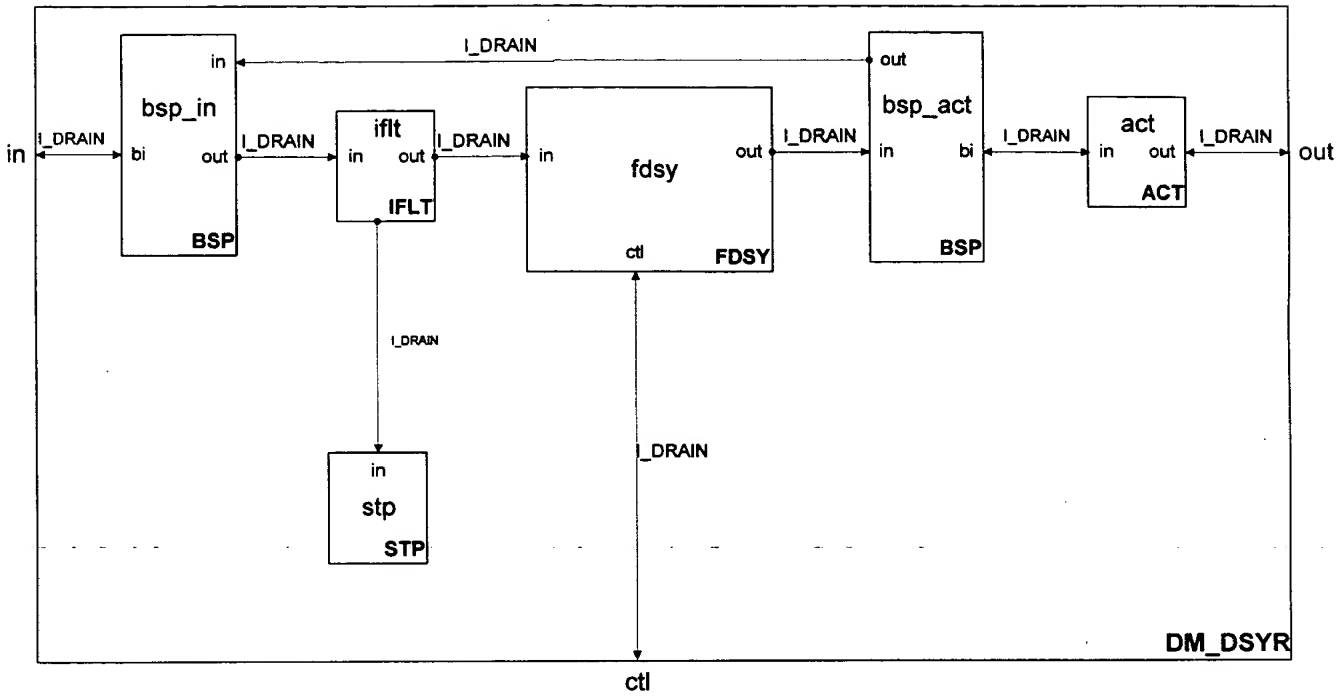

I_DRAIN
in
bsp_in
bi
out
BSP
I_DRAIN
iflt
in
out
IFLT
I_DRAIN
in
fdsy
out
ctl
FDSY
I_DRAIN
out
bsp_act
in
bi
BSP
I_DRAIN
act
in
out
ACT
I_DRAIN
out
I_DRAIN
in
stp
STP
I_DRAIN
DM_DSYR
ctl

Fig. 84

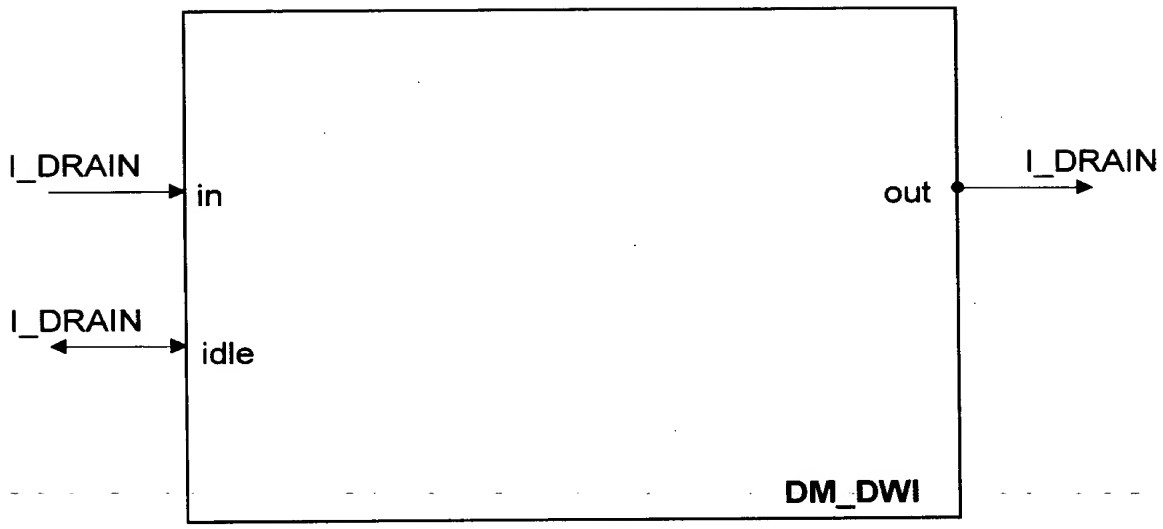


Fig. 85

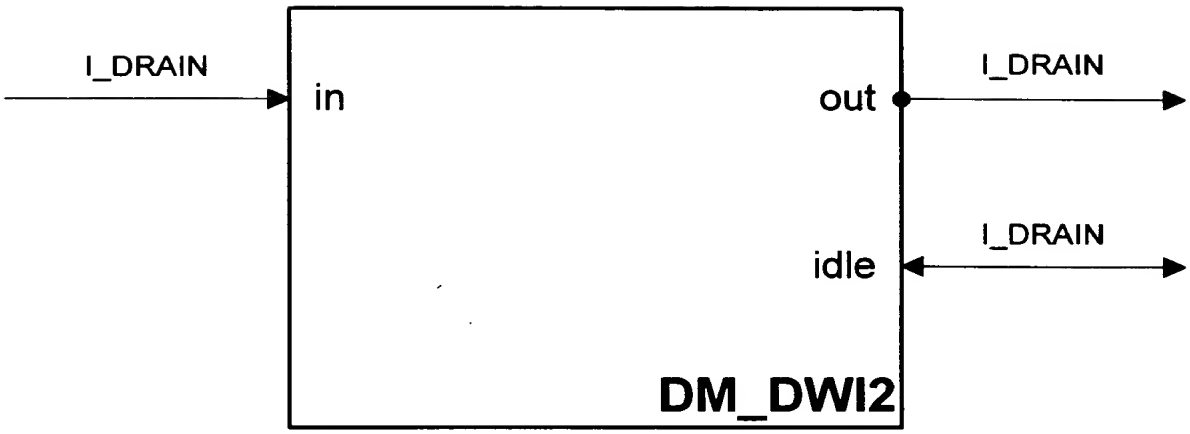


Fig. 86

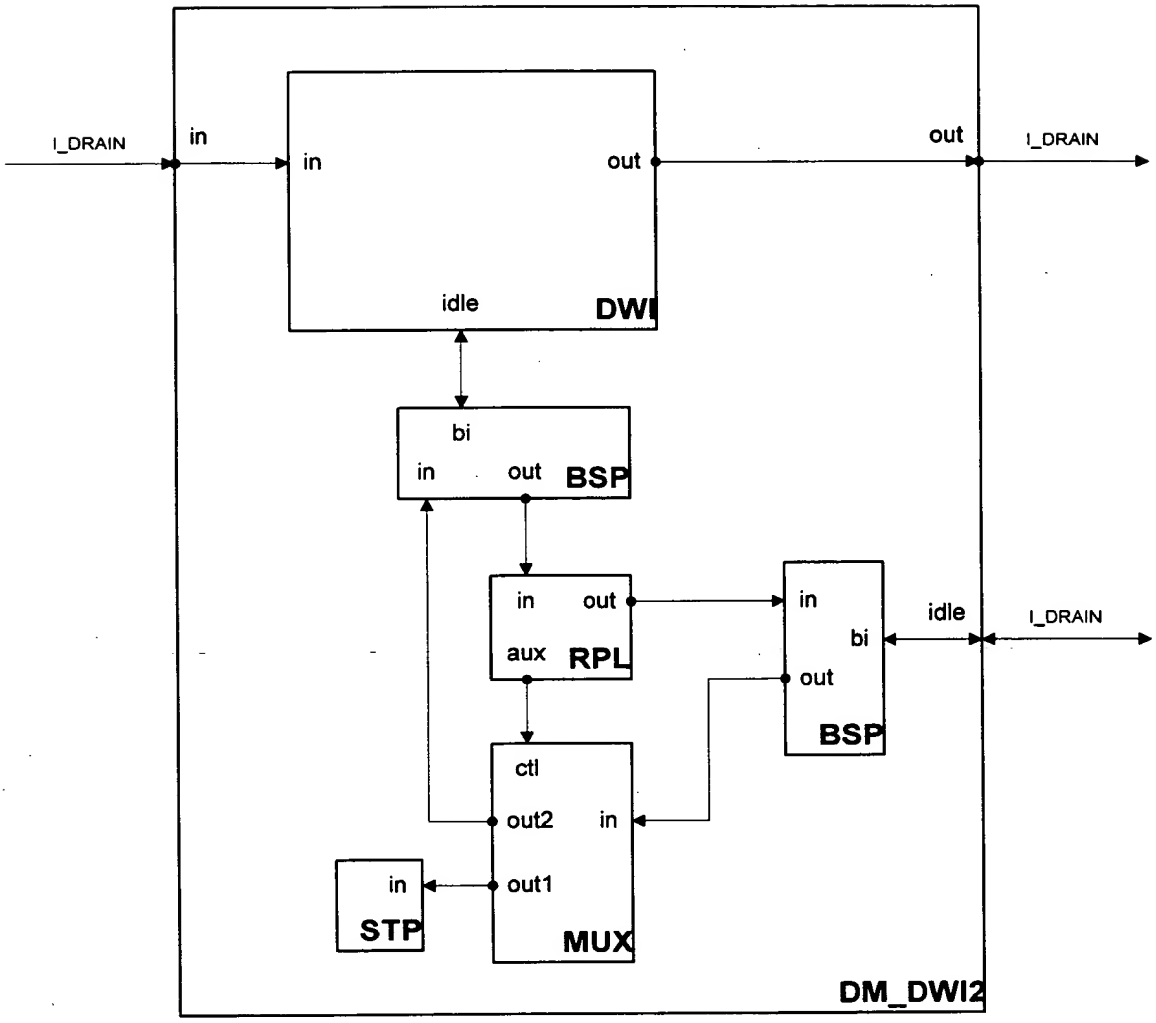

I_DRAIN
in
in
out
out
I_DRAIN
idle
DWI
bi
in
out
BSP
in
out
aux
RPL
in
bi
out
BSP
idle
I_DRAIN
ctl
out2
in
in
out1
STP
MUX
DM_DWI2

Fig. 87

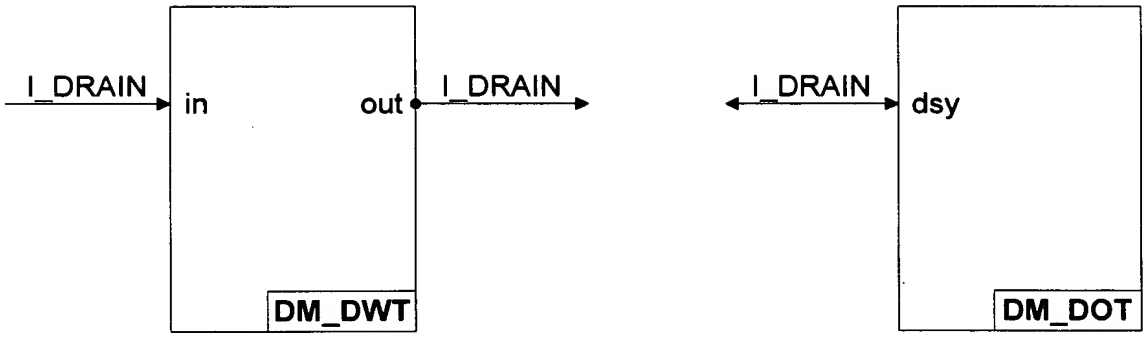


Fig. 88

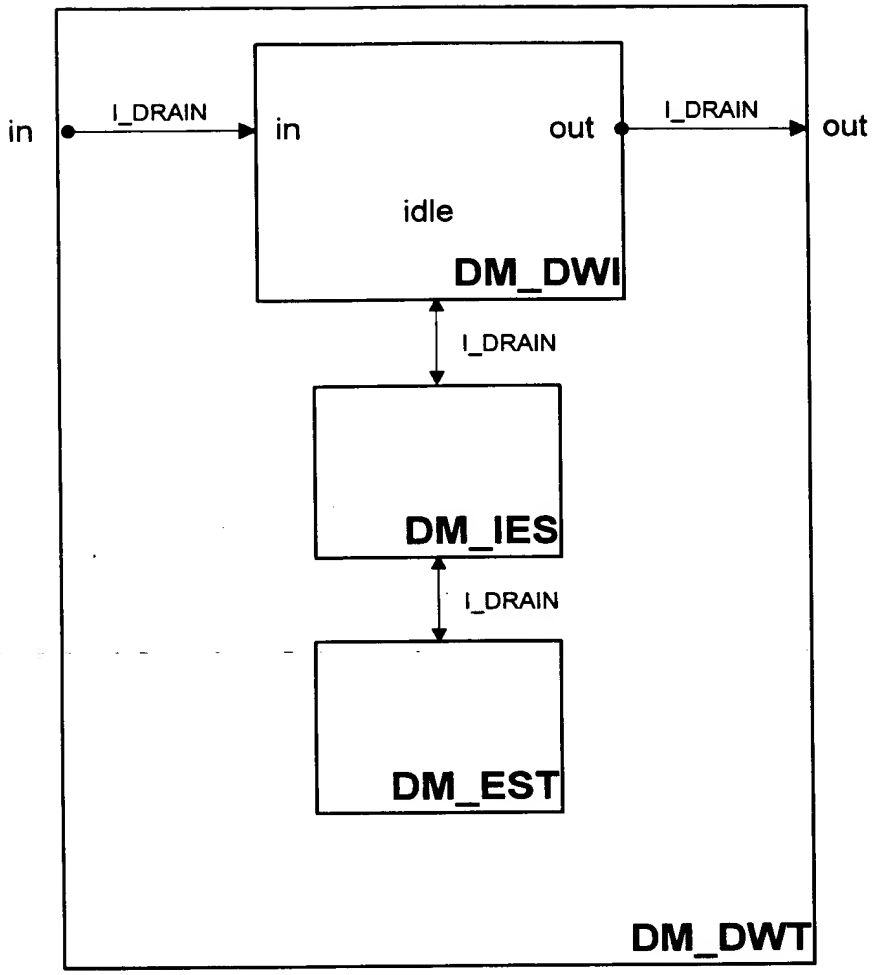

in
I_DRAIN
in
out
I_DRAIN
out
idle
DM_DWI
I_DRAIN
DM_IES
I_DRAIN
DM_EST
DM_DWT

Fig. 89

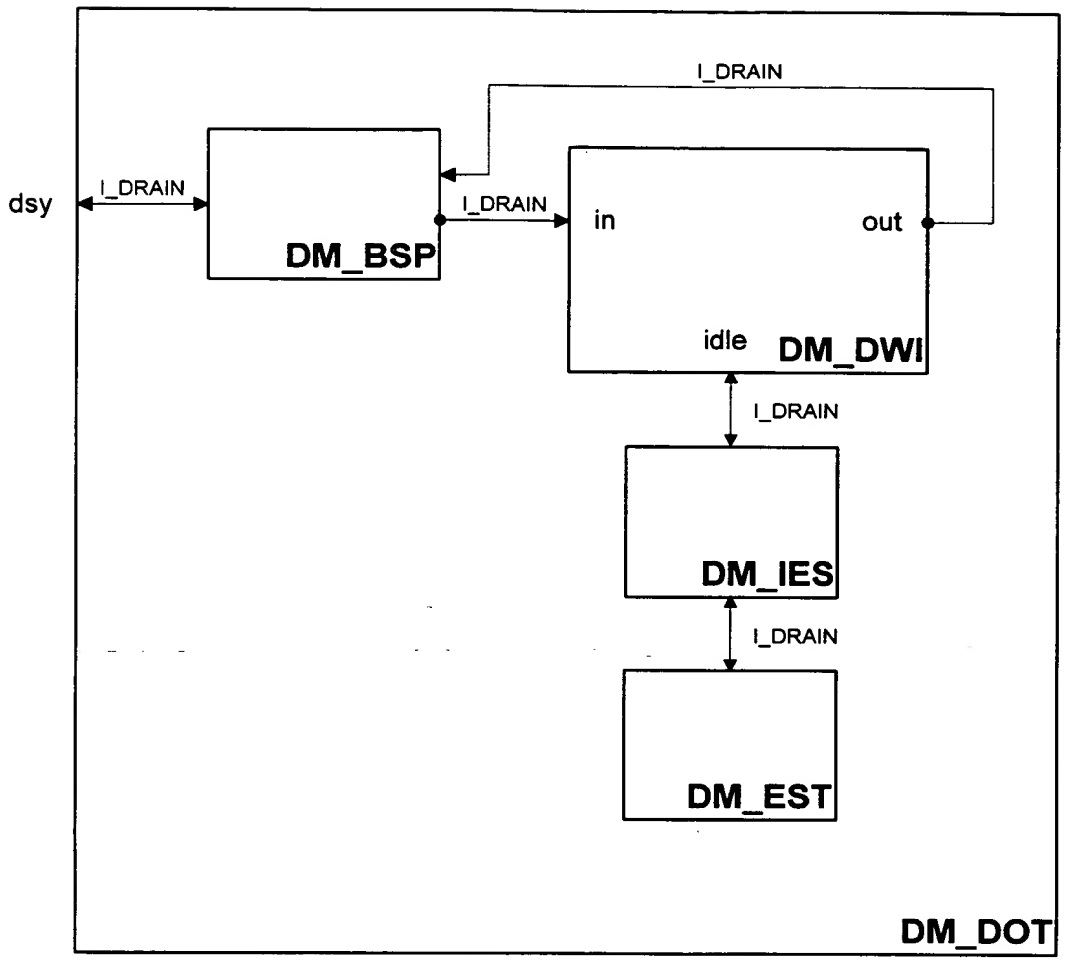

I_DRAIN
dsy
I_DRAIN
DM_BSP
I_DRAIN
in
out
idle
DM_DWI
I_DRAIN
DM_IES
I_DRAIN
DM_EST
DM_DOT

Fig. 90

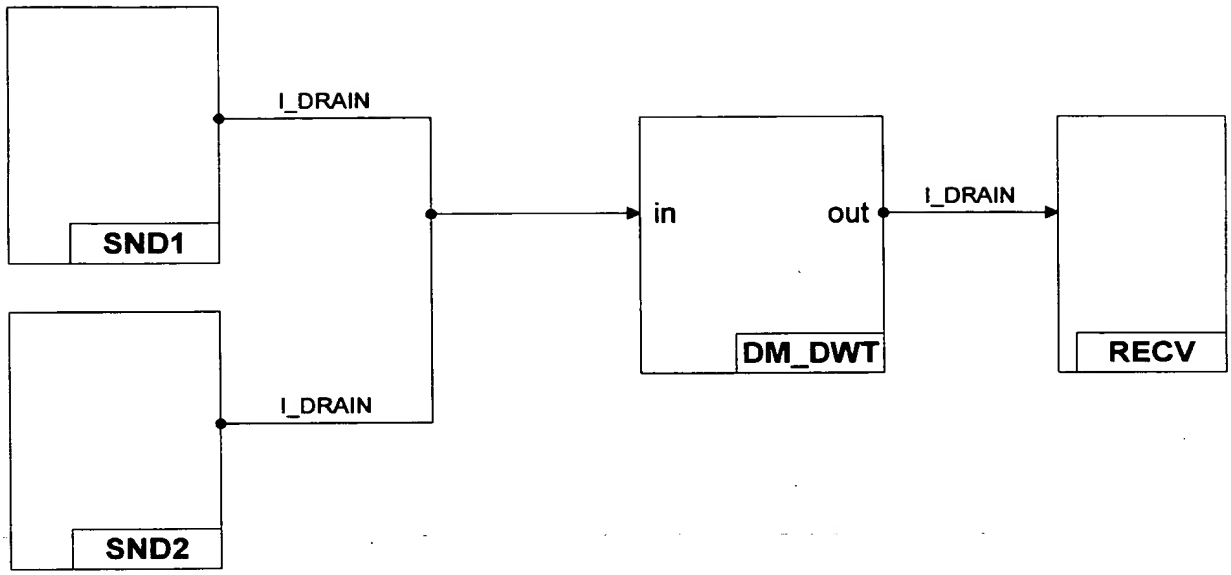


Fig. 91

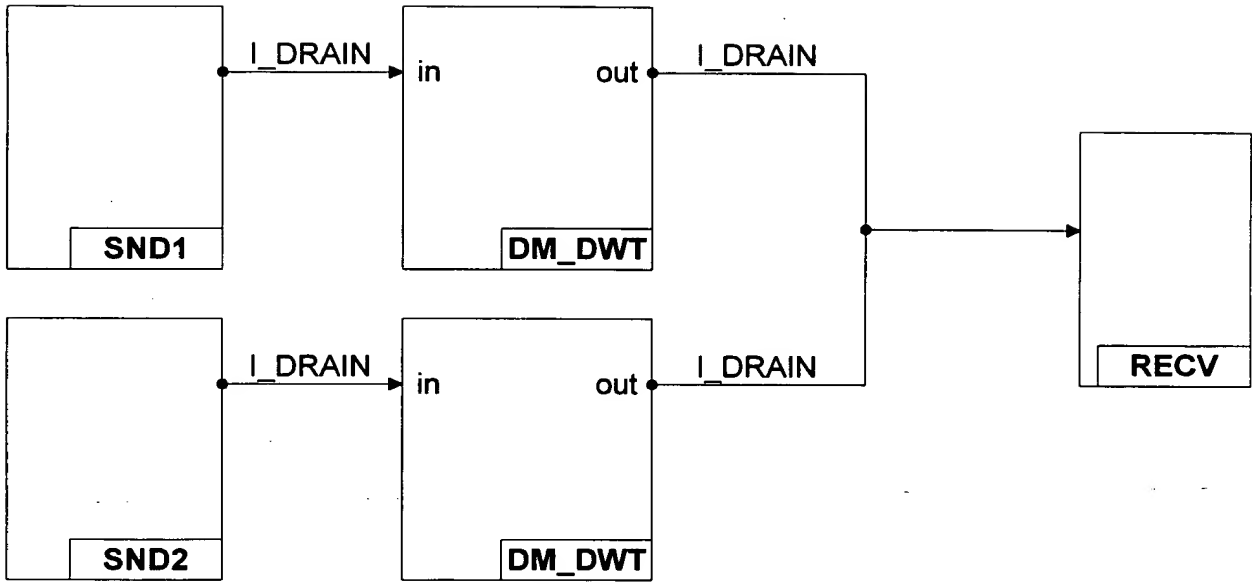

I_DRAIN
in
out
I_DRAIN
SND1
DM_DWT
I_DRAIN
in
out
I_DRAIN
SND2
DM_DWT
RECV

Fig. 92

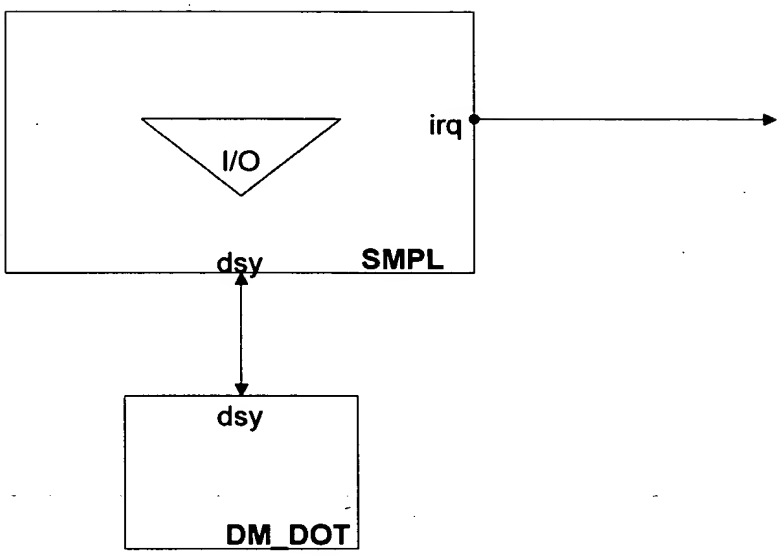


Fig. 93

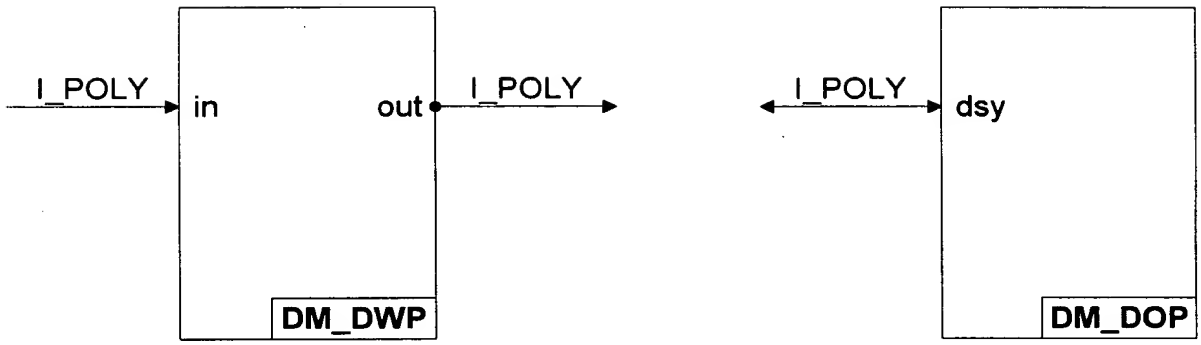


Fig. 94

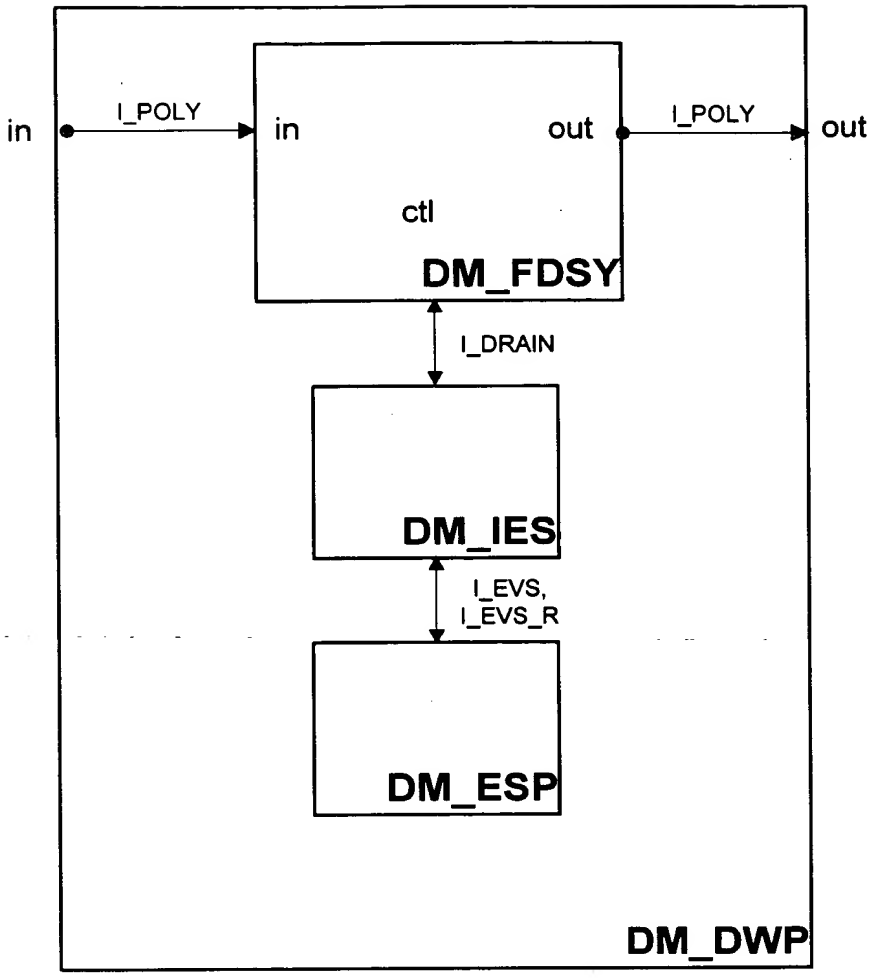

in
I_POLY
in
out
I_POLY
out
ctl
DM_FDSY
I_DRAIN
DM_IES
I_EVS,
I_EVS_R
DM_ESP
DM_DWP

Fig. 95

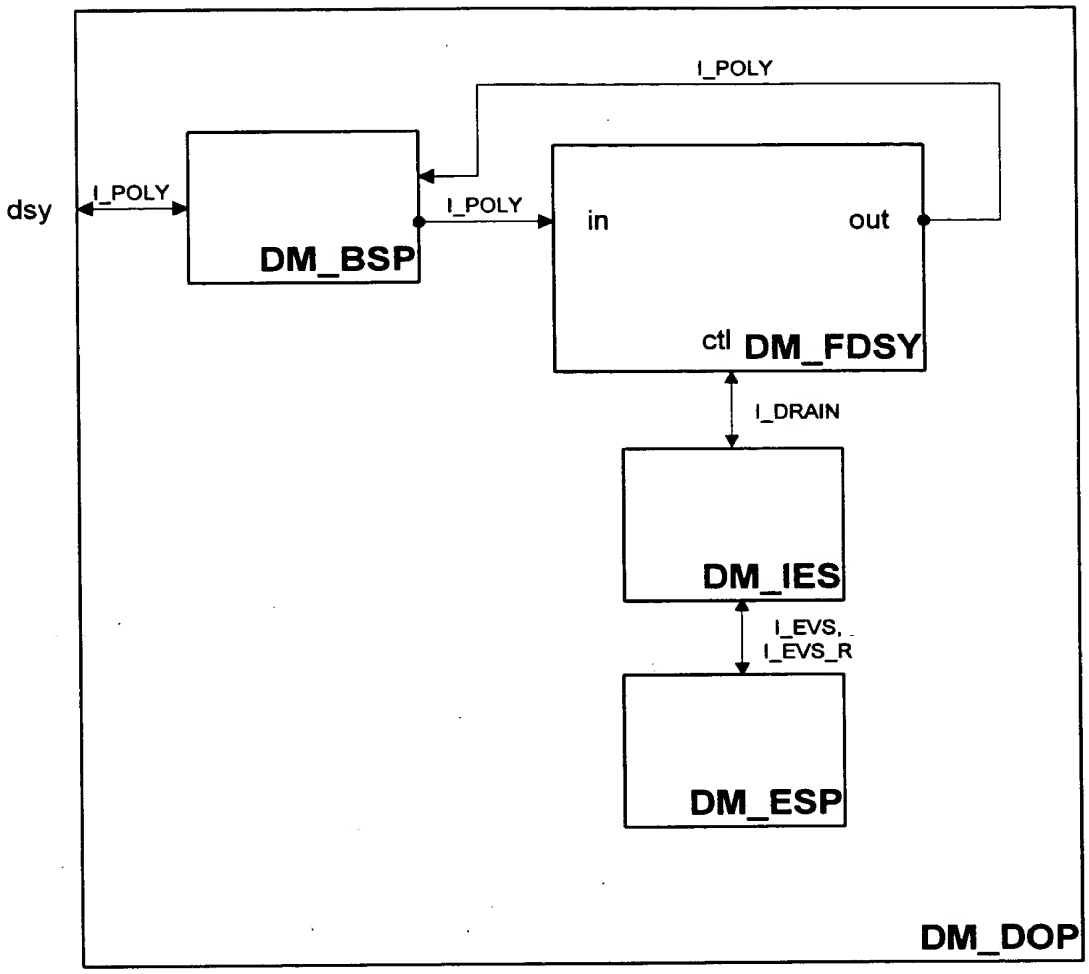

I_POLY
dsy
I_POLY
I_POLY
DM_BSP
in
out
ctl
DM_FDSY
I_DRAIN
DM_IES
I_EVS,
I_EVS_R
DM_ESP
DM_DOP

Fig. 96

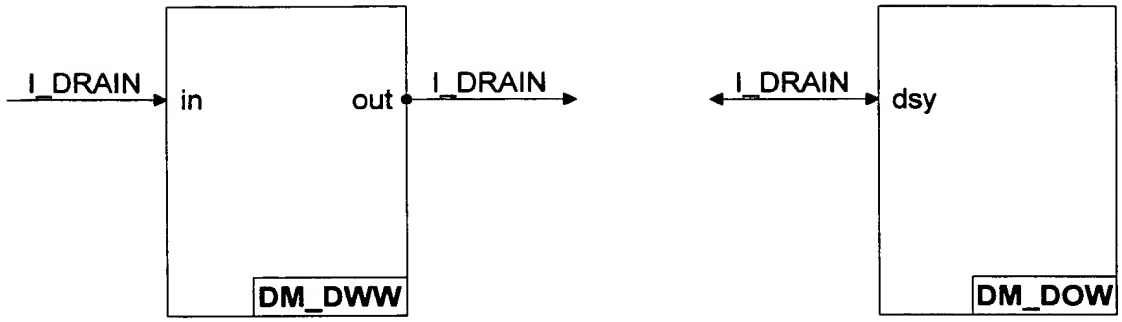


Fig. 97

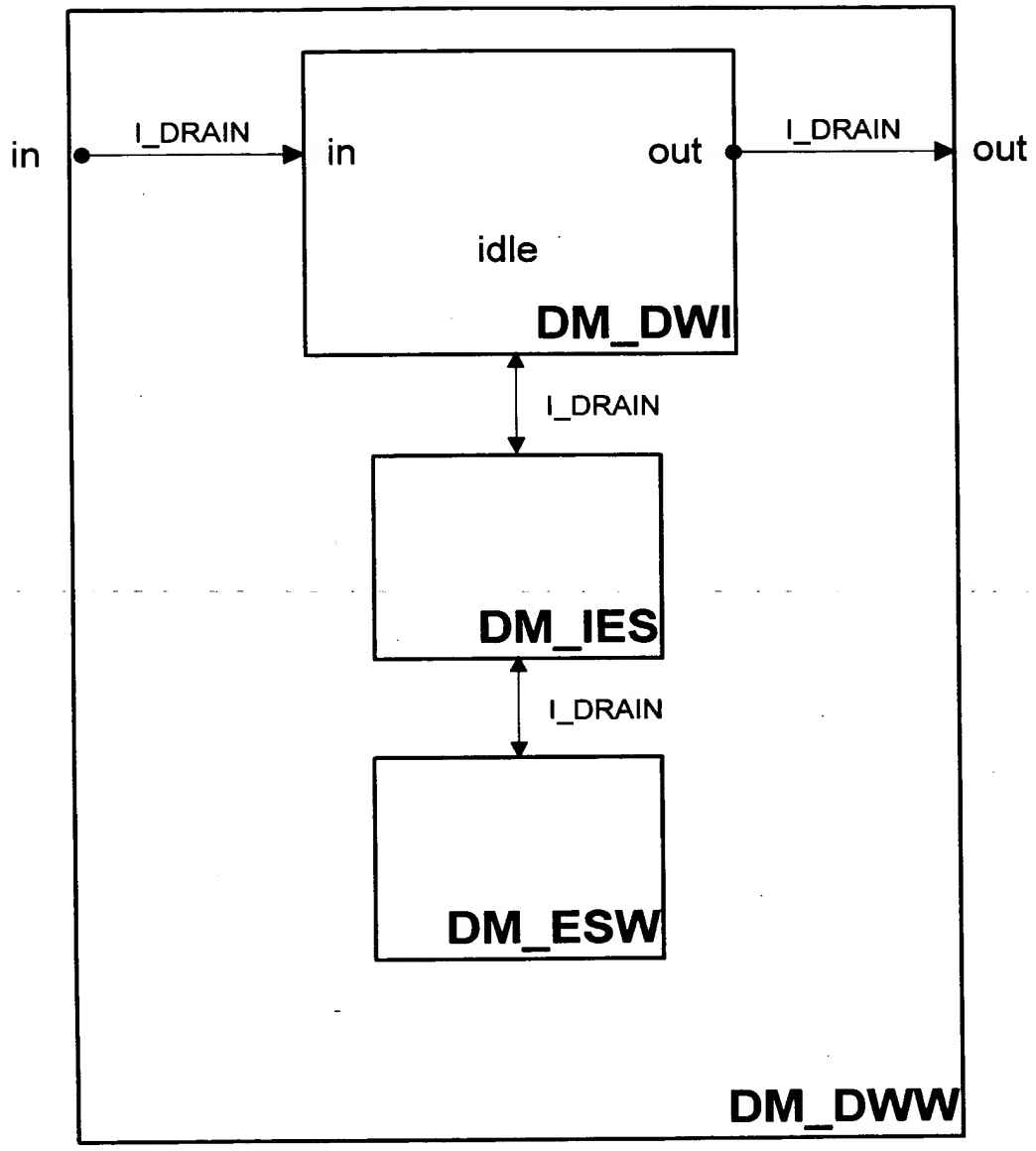

in
I_DRAIN
in
out
I_DRAIN
out
idle
DM_DWI
I_DRAIN
DM_IES
I_DRAIN
DM_ESW
DM_DWW

Fig. 98

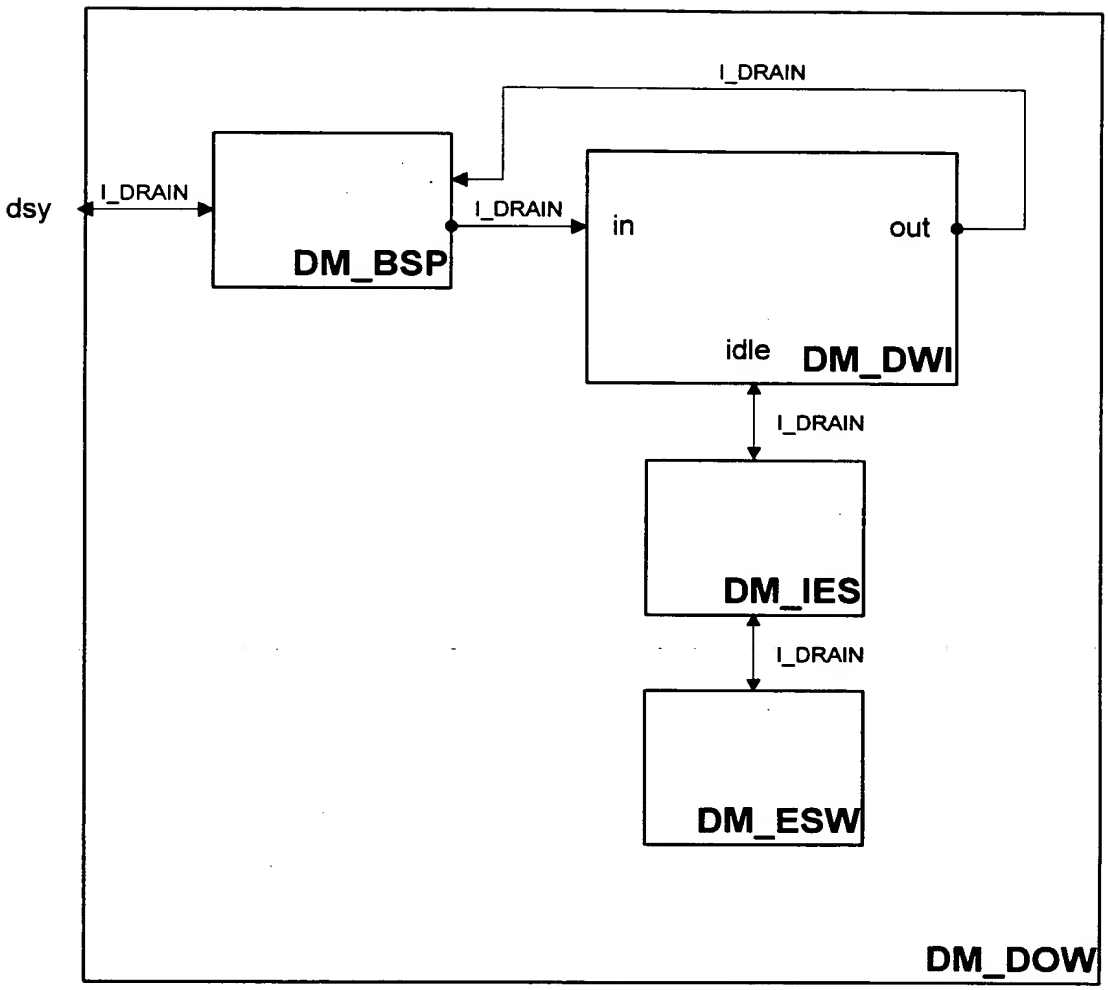

I_DRAIN
dsy
I_DRAIN
DM_BSP
I_DRAIN
in
out
idle
DM_DWI
I_DRAIN
DM_IES
I_DRAIN
DM_ESW
DM_DOW

Fig. 99

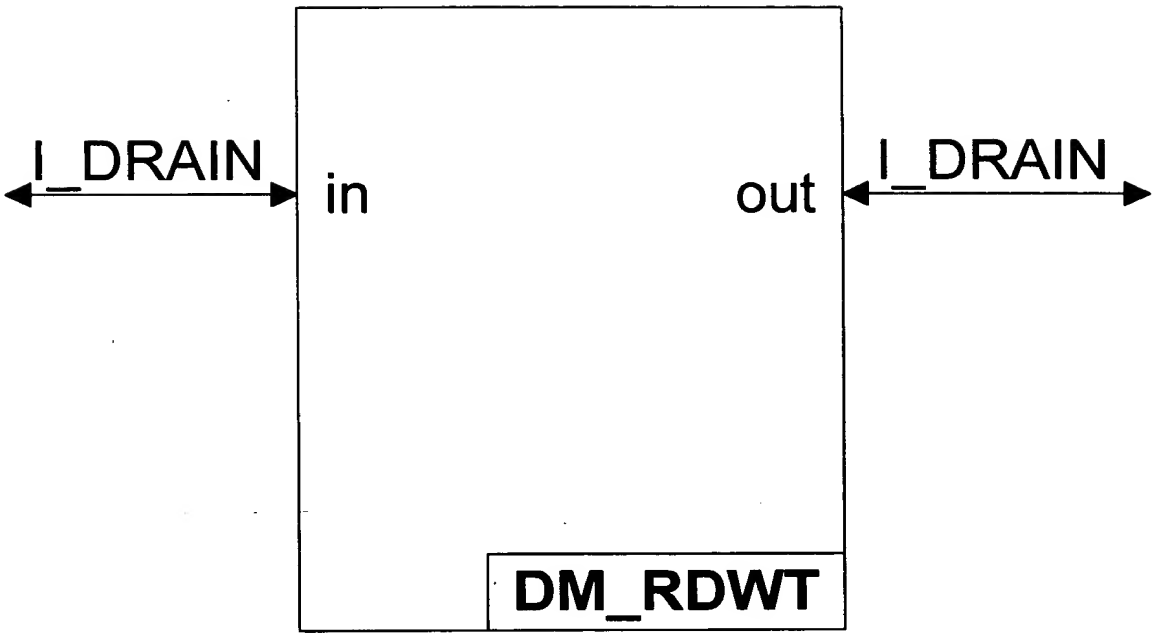


Fig. 100

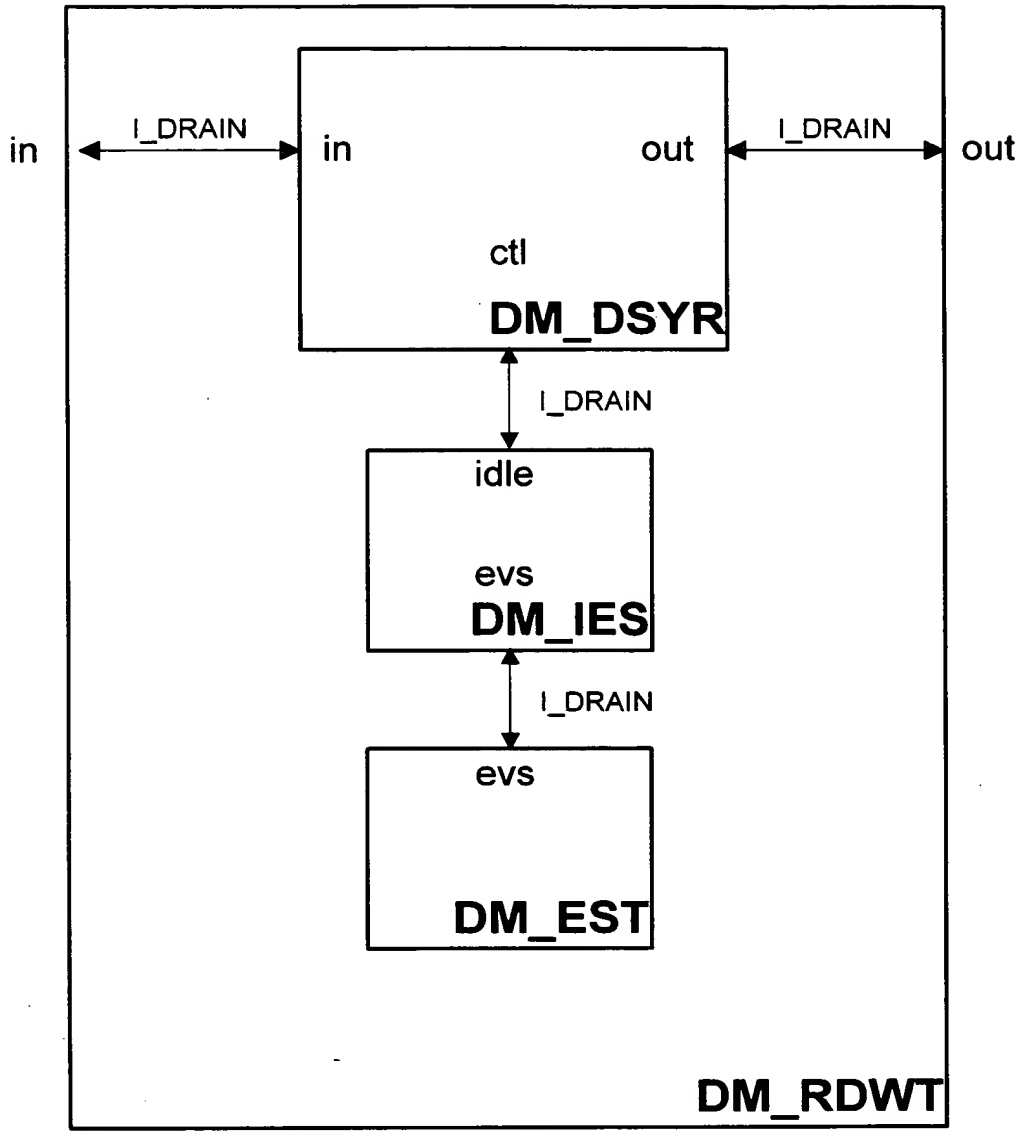

in
I_DRAIN
in
out
I_DRAIN
out
ctl
DM_DSYR
I_DRAIN
idle
evs
DM_IES
I_DRAIN
evs
DM_EST
DM_RDWT

Fig. 101

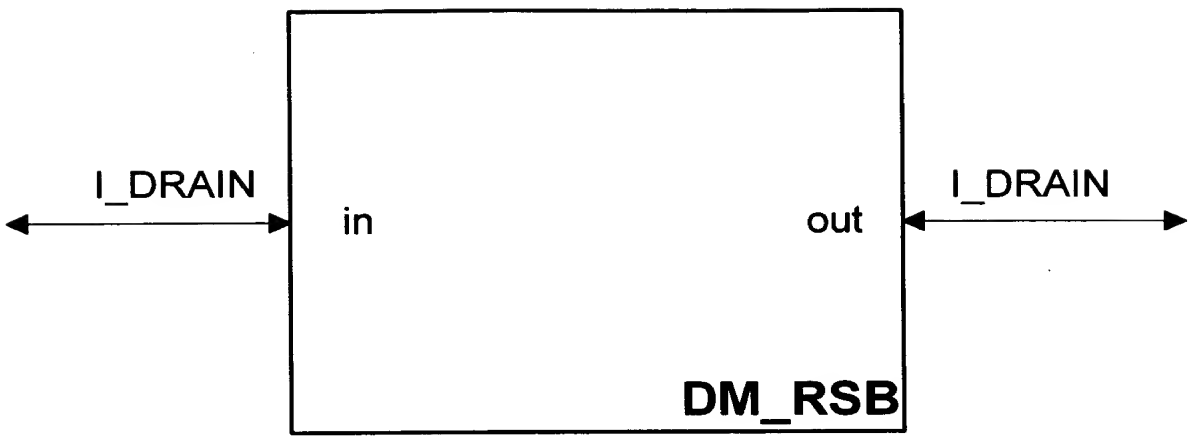


Fig. 102

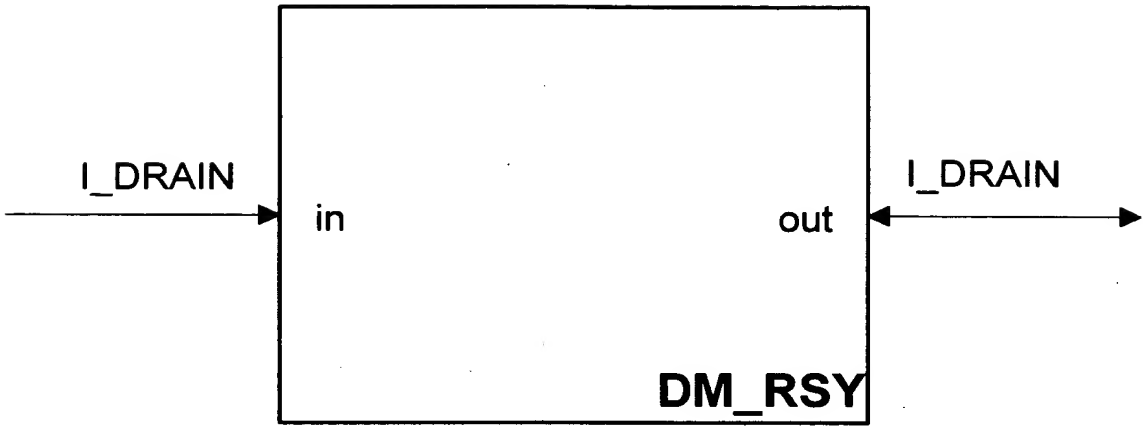


Fig. 103

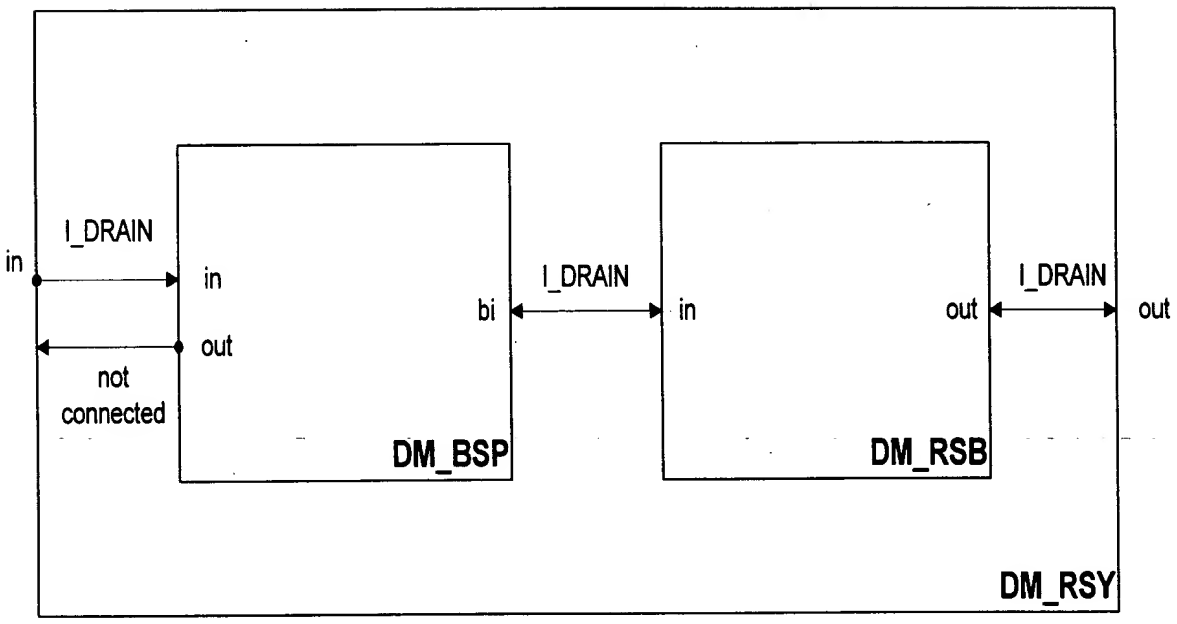

in
I_DRAIN
in
out
not
connected
DM_BSP
bi
I_DRAIN
in
out
DM_RSB
I_DRAIN
out
DM_RSY

Fig. 104

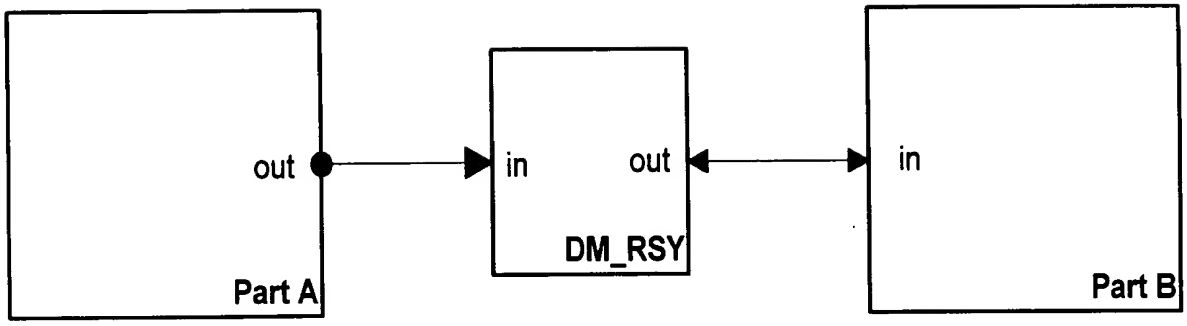


Fig. 105

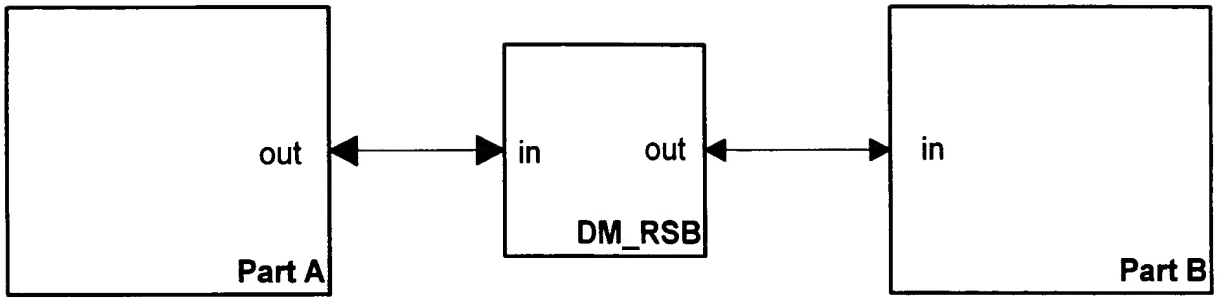


Fig. 106

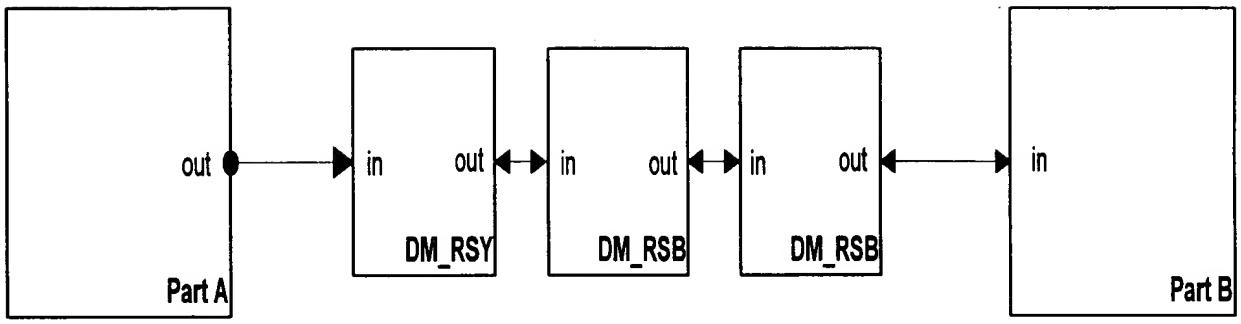


Fig. 107

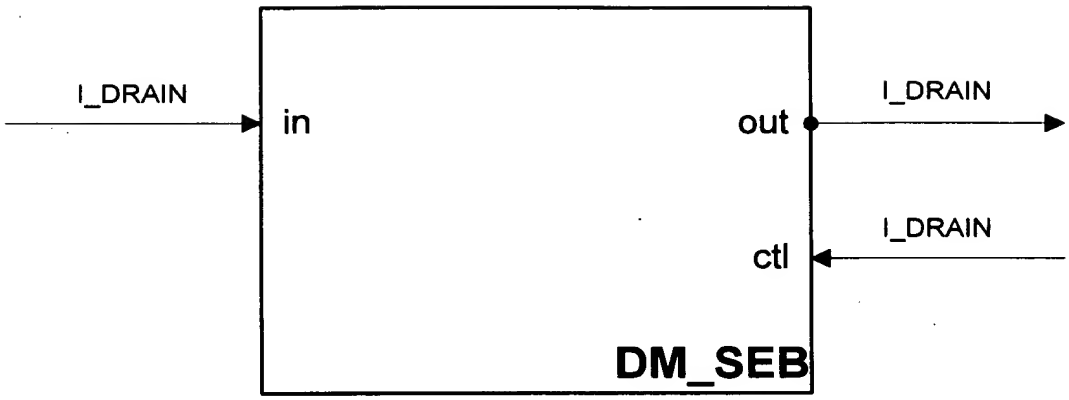


Fig. 108

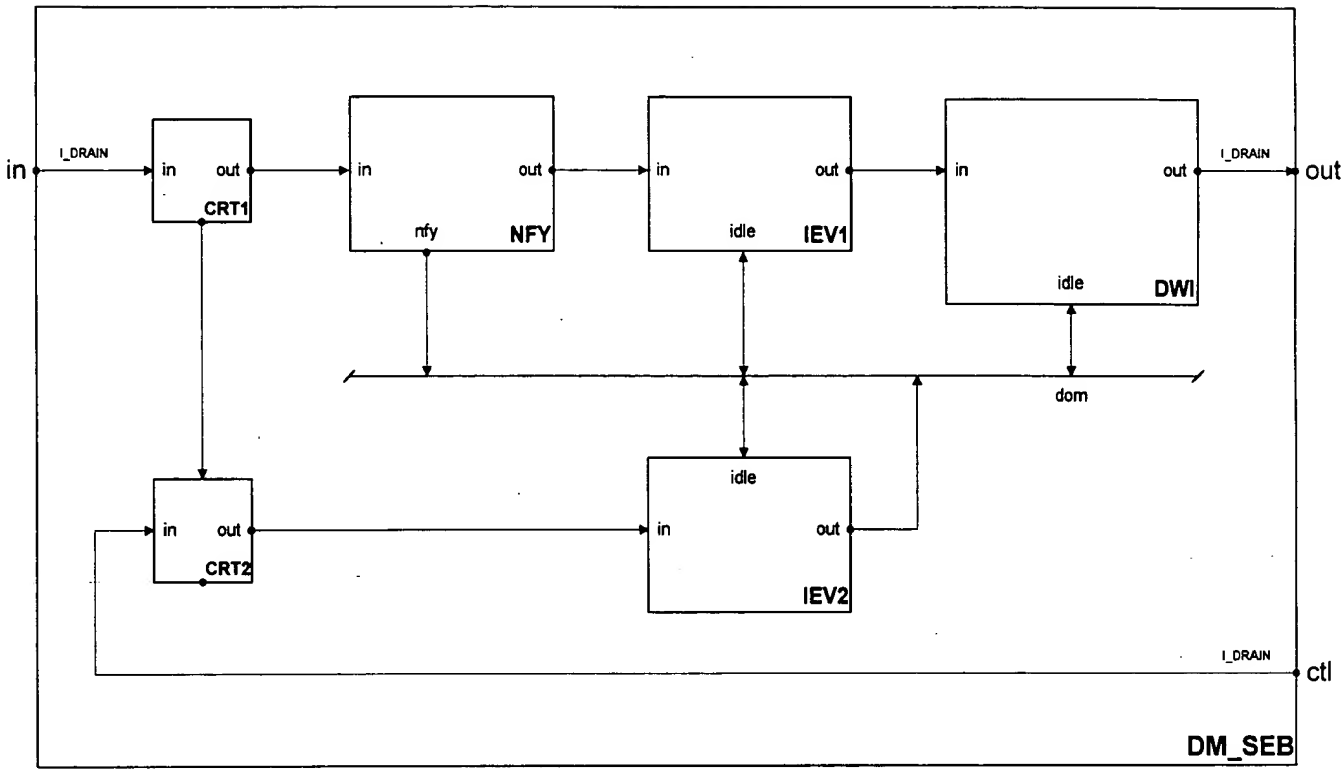

in
I_DRAIN
in
out
CRT1
in
out
nfy
NFY
in
out
idle
IEV1
in
out
idle
DWI
I_DRAIN
out
dom
idle
in
out
CRT2
in
out
IEV2
I_DRAIN
ctl
DM_SEB

Fig. 109

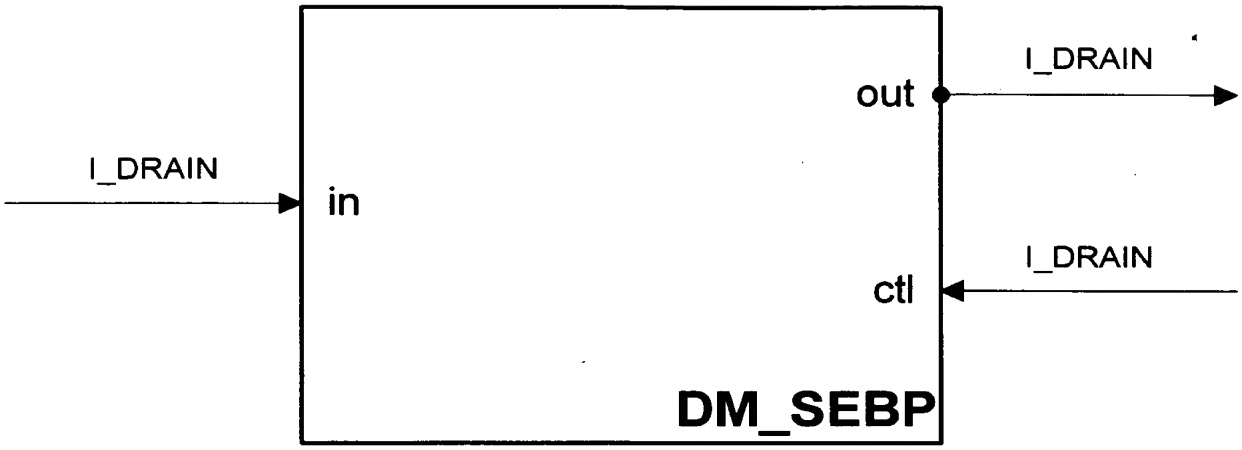


Fig. 110

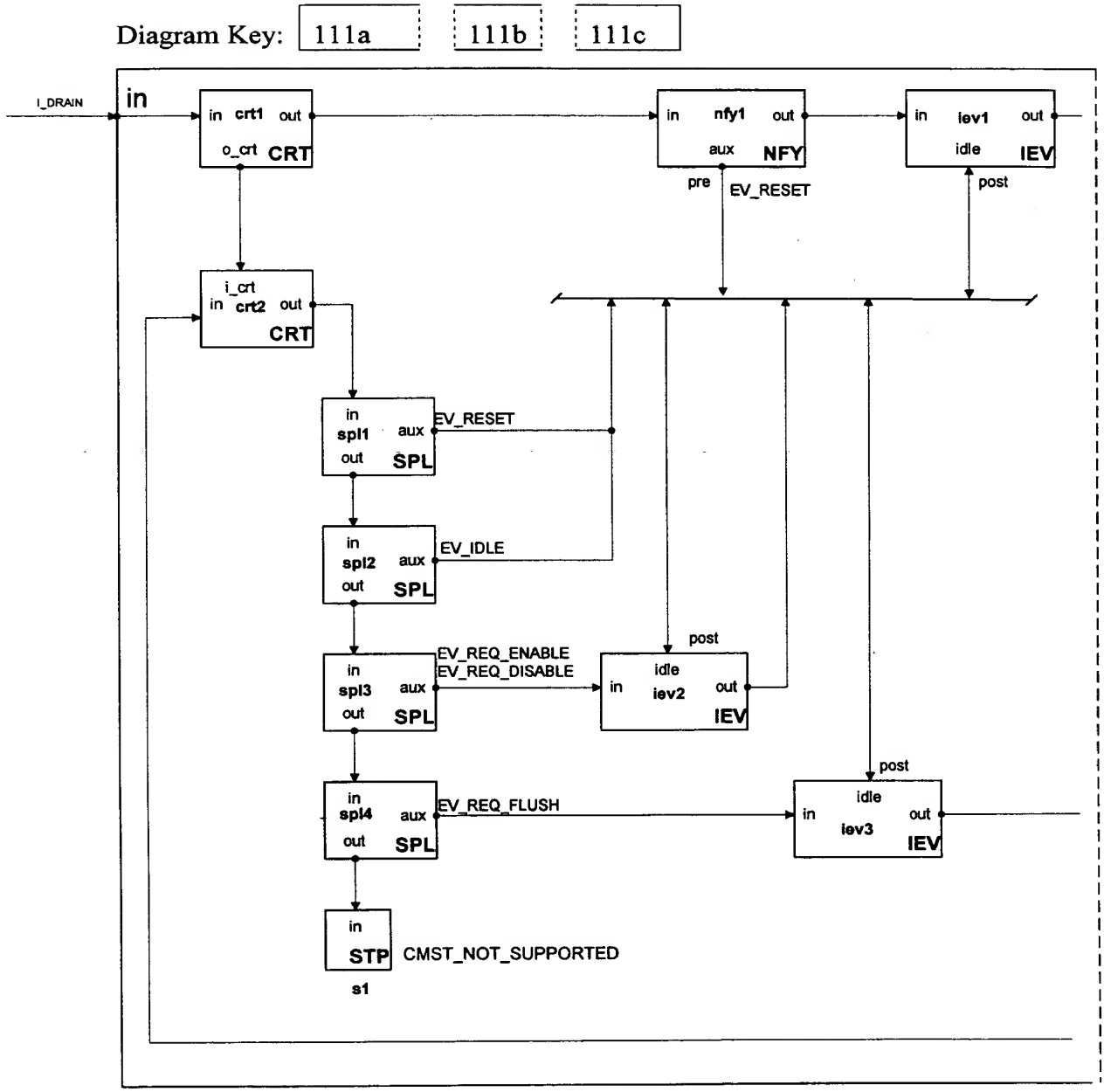


Diagram Key:
111a
111b
111c
I_DRAIN
in
in crt1 out
o_crt CRT
in nfy1 out
aux NFY
pre
EV_RESET
in iev1 out
idle IEV
post
i_crt
in crt2 out
CRT
in
spl1 aux
out SPL
EV_RESET
in
spl2 aux
out SPL
EV_IDLE
in
spl3 aux
out SPL
EV_REQ_ENABLE
EV_REQ_DISABLE
post
idle
in iev2 out
IEV
in
spl4 aux
out SPL
EV_REQ_FLUSH
post
idle
in iev3 out
IEV
in
STP
CMST_NOT_SUPPORTED
s1

Fig. 111a

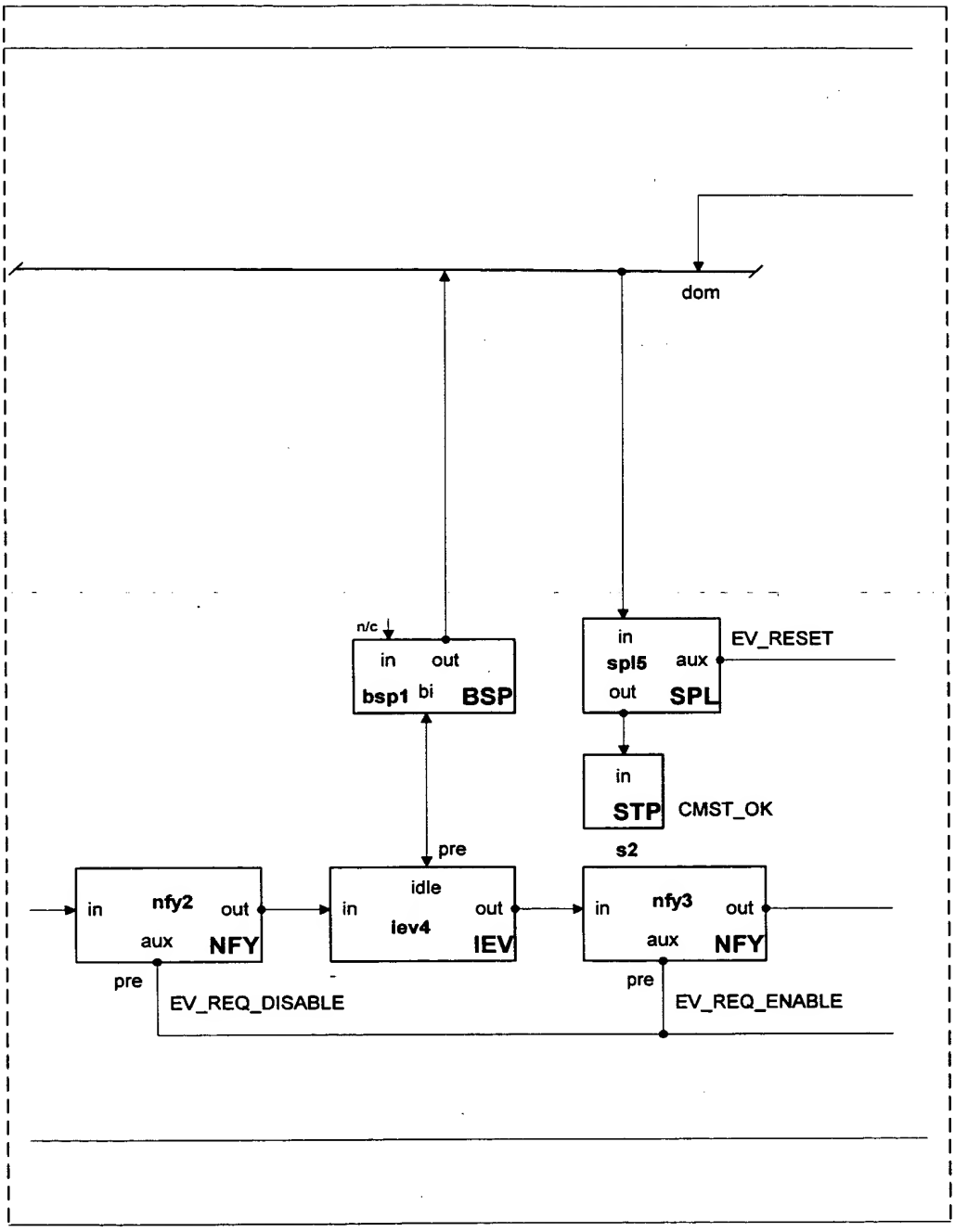

dom
n/c
in
out
bsp1
bi
BSP
in
spl5
aux
out
SPL
EV_RESET
in
STP
CMST_OK
pre
s2
in
nfy2
out
aux
NFY
pre
EV_REQ_DISABLE
idle
in
out
iev4
IEV
in
nfy3
out
aux
NFY
pre
EV_REQ_ENABLE

Fig. 111b

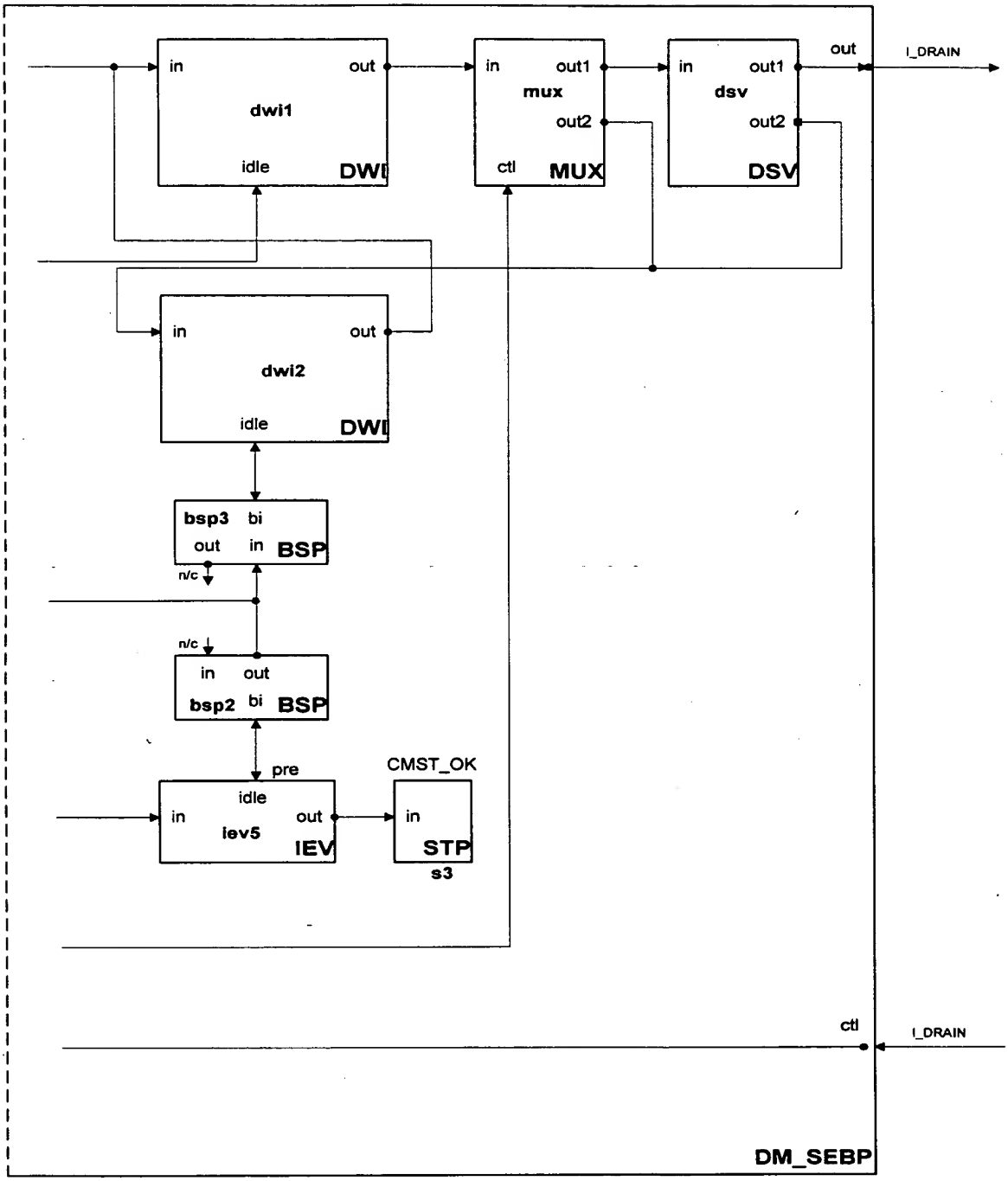

in
out
dwi1
idle
DWI
in
out1
mux
out2
ctl
MUX
in
out1
dsv
out2
DSV
out
I_DRAIN
in
out
dwi2
idle
DWI
bsp3 bi
out in
BSP
n/c
n/c
in out
bsp2 bi
BSP
pre
idle
in
out
iev5
IEV
CMST_OK
in
STP
s3
ctl
I_DRAIN
DM_SEBP

Fig. 111c

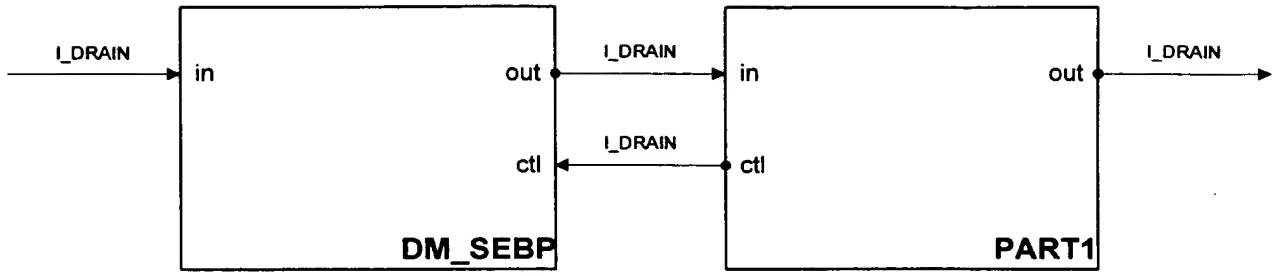

I_DRAIN
in
out
I_DRAIN
I_DRAIN
ctl
DM_SEBP
in
out
I_DRAIN
ctl
PART1

Fig. 112

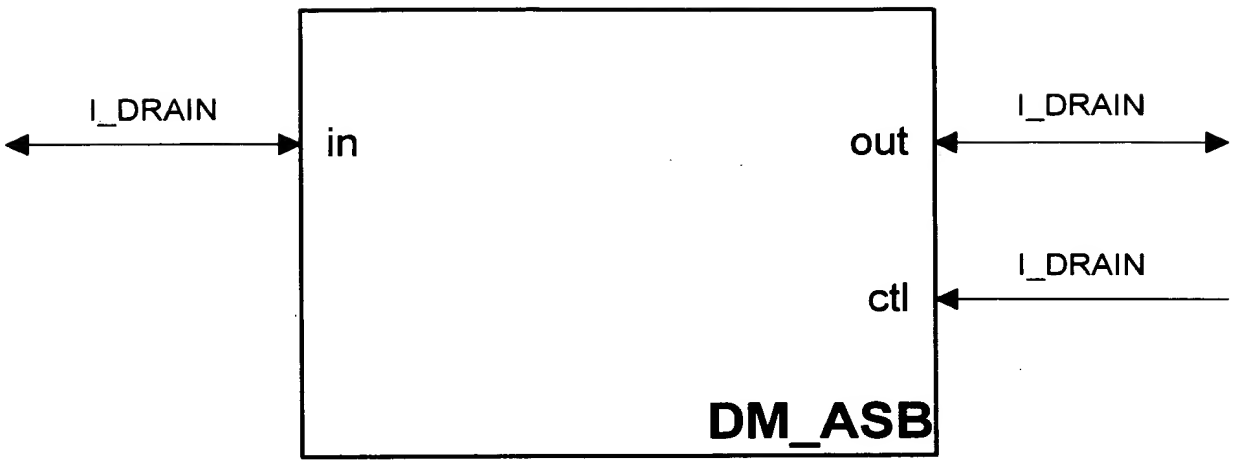


Fig. 113

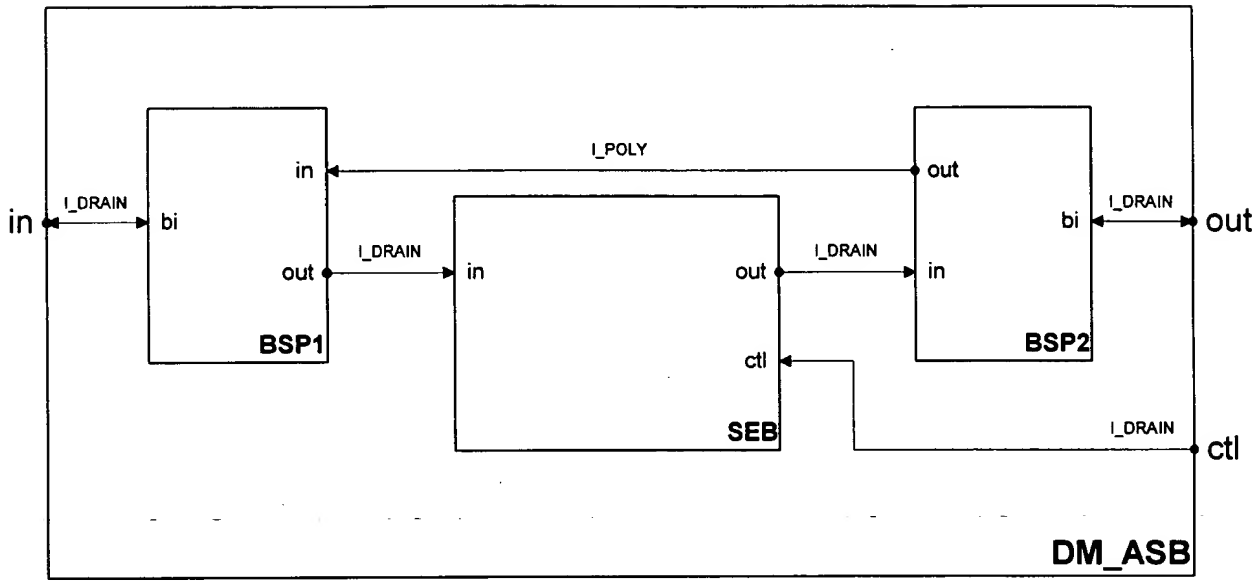

in
I_DRAIN
bi
in
out
BSP1
I_DRAIN
I_POLY
in
out
SEB
ctl
I_DRAIN
out
in
BSP2
bi
I_DRAIN
out
I_DRAIN
ctl
DM_ASB

Fig. 114

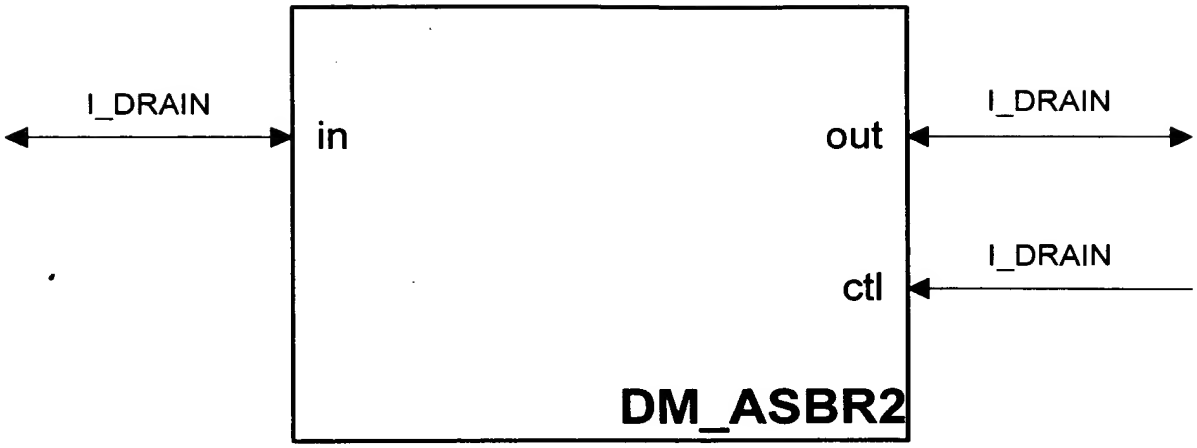


Fig. 115

Diagram Key: 116a 116b

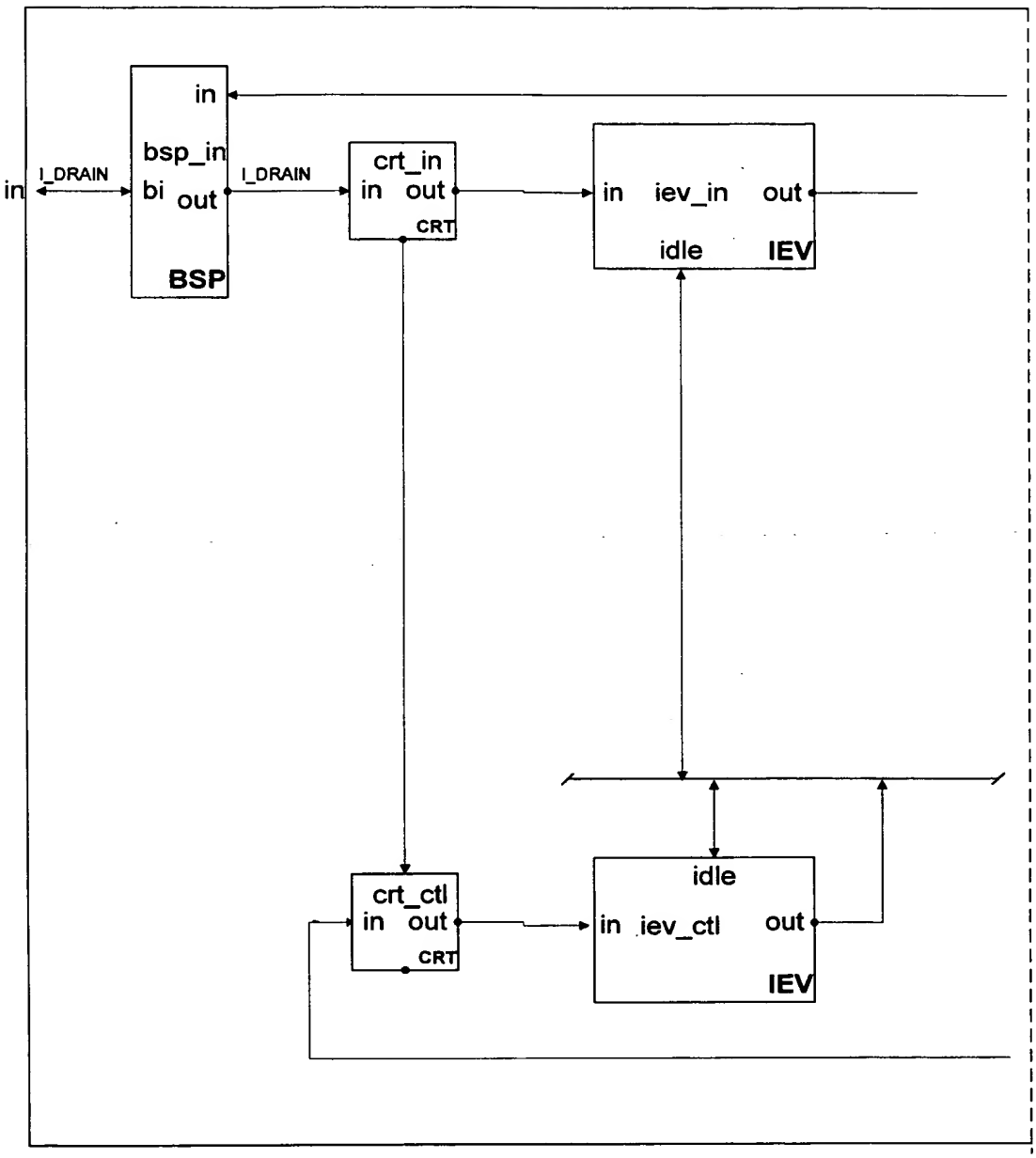


Fig. 116a

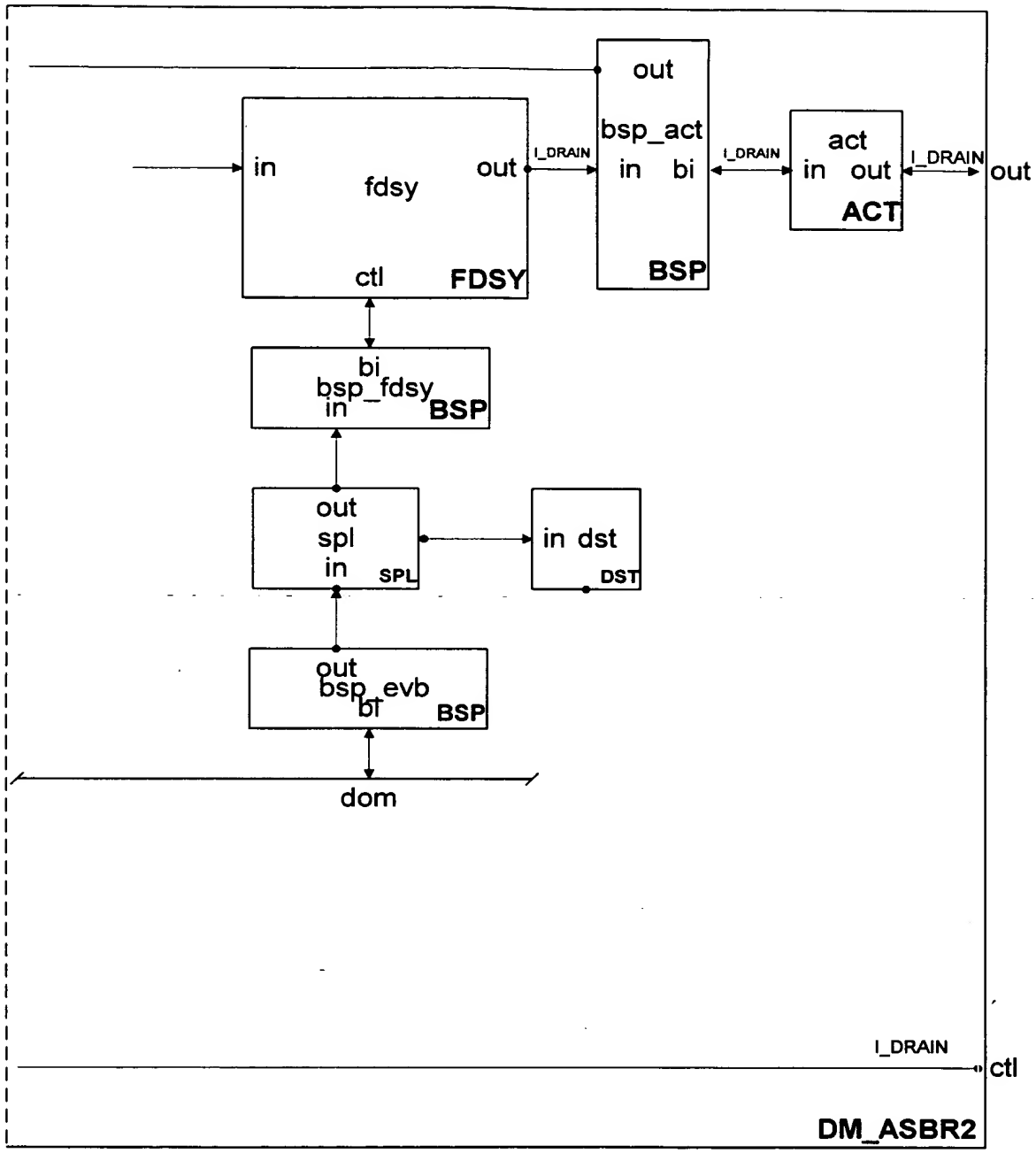

out
bsp_act
in bi
BSP
I_DRAIN
I_DRAIN
act
in out
ACT
I_DRAIN
out
in
fdsy
out
ctl
FDSY
bi
bsp_fdsy
in
BSP
out
spl
in
SPL
in dst
DST
out
bsp_evb
bi
BSP
dom
I_DRAIN
ctl
DM_ASBR2

Fig. 116b

Diagram Key: 117a 117b

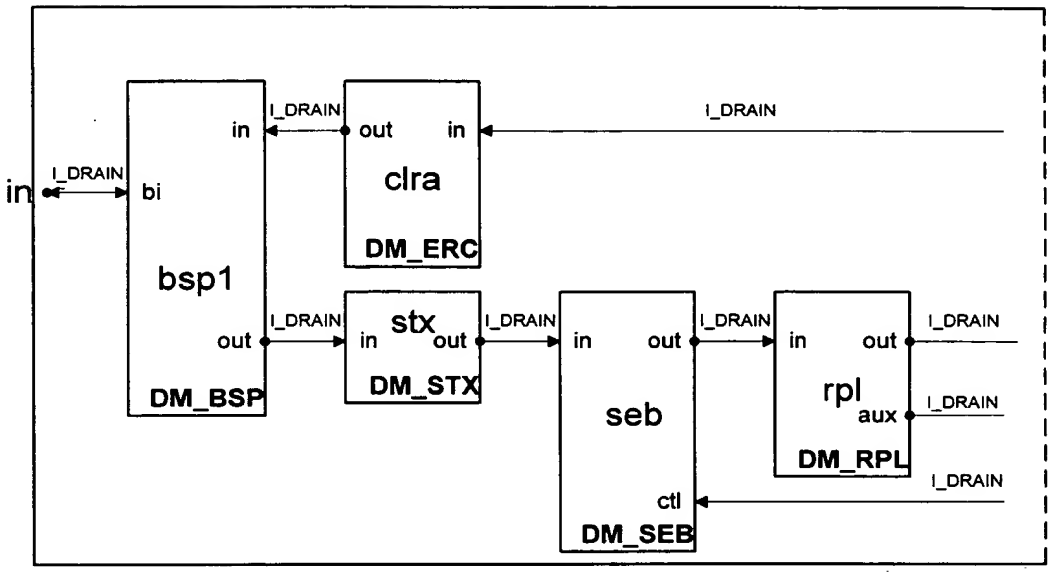


Fig. 117a

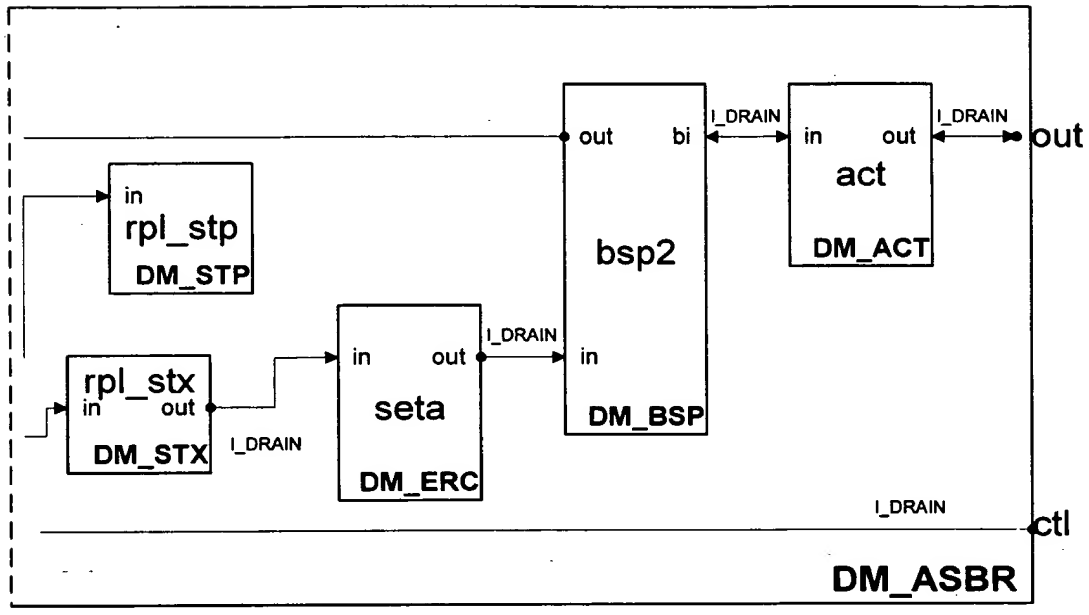

out
bi
I_DRAIN
in
out
act
DM_ACT
I_DRAIN
out
in
rpl_stp
DM_STP
bsp2
in
rpl_stx
in
out
DM_STX
I_DRAIN
in
out
seta
DM_ERC
I_DRAIN
in
DM_BSP
I_DRAIN
ctl
DM_ASBR

Fig. 117b

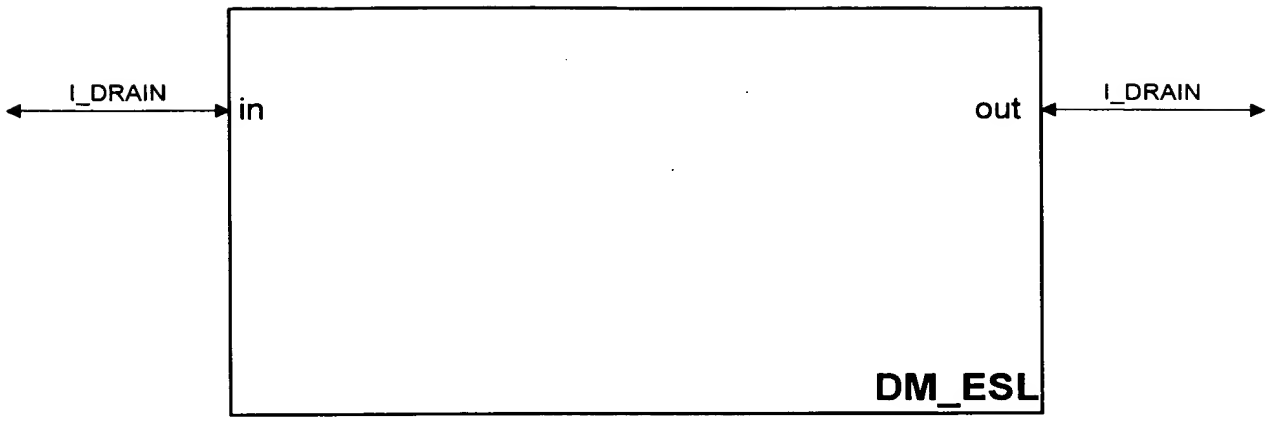


Fig. 118

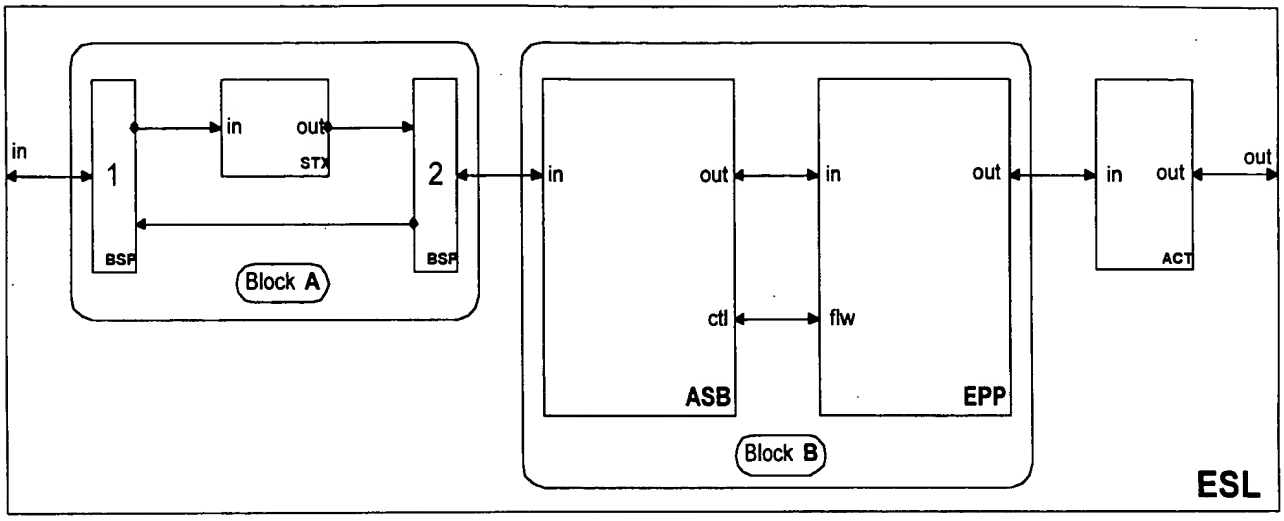

in
1
BSP
in
out
STX
2
BSP
Block A
in
out
ctl
ASB
in
out
flw
EPP
Block B
in
out
ACT
out
ESL

Fig. 119

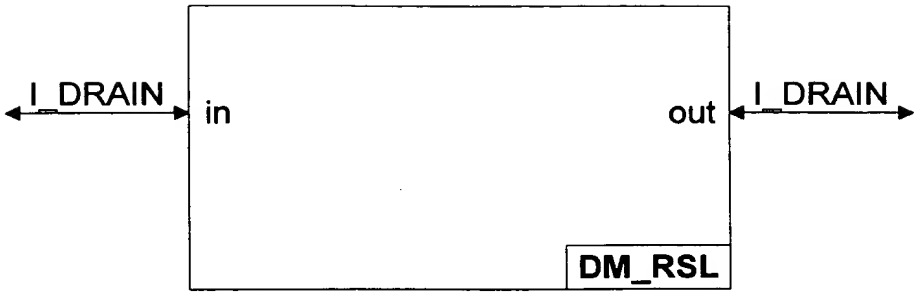
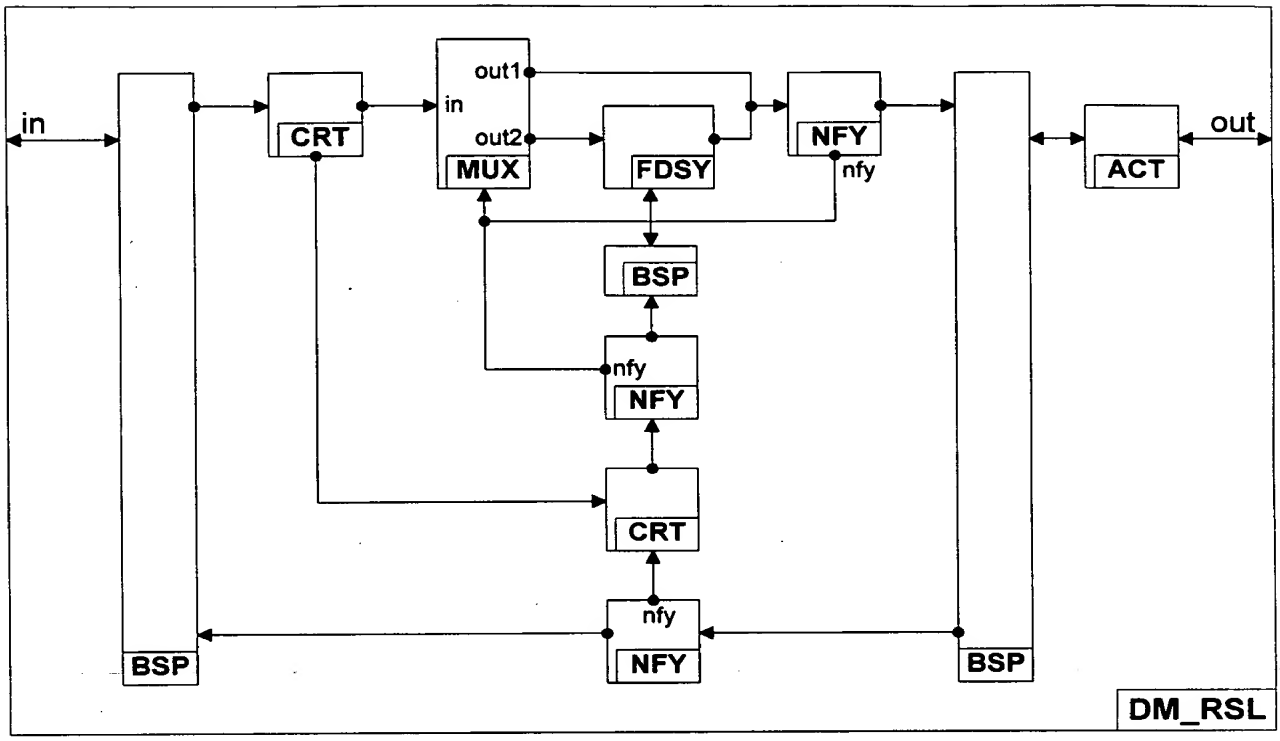


Fig. 120



Note: all connections are I_DRAIN type

Fig. 121

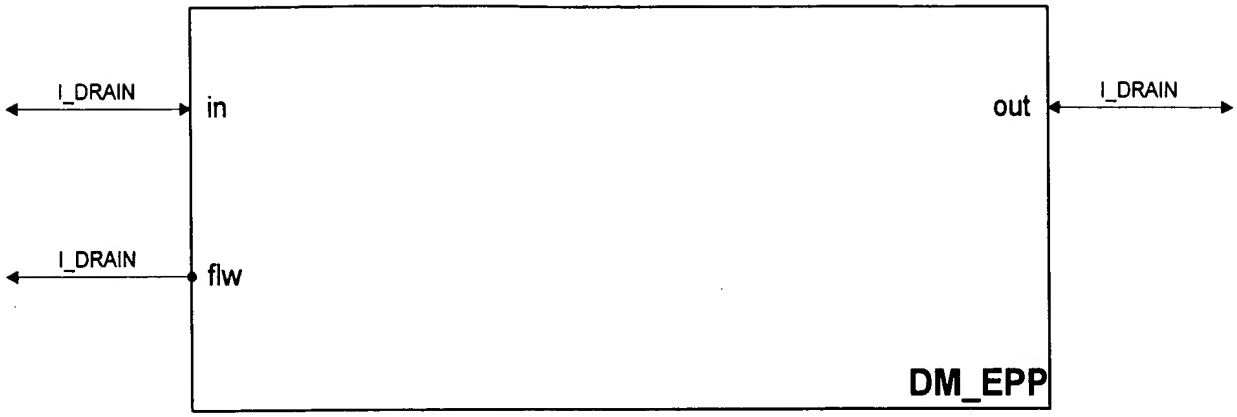


Fig. 122

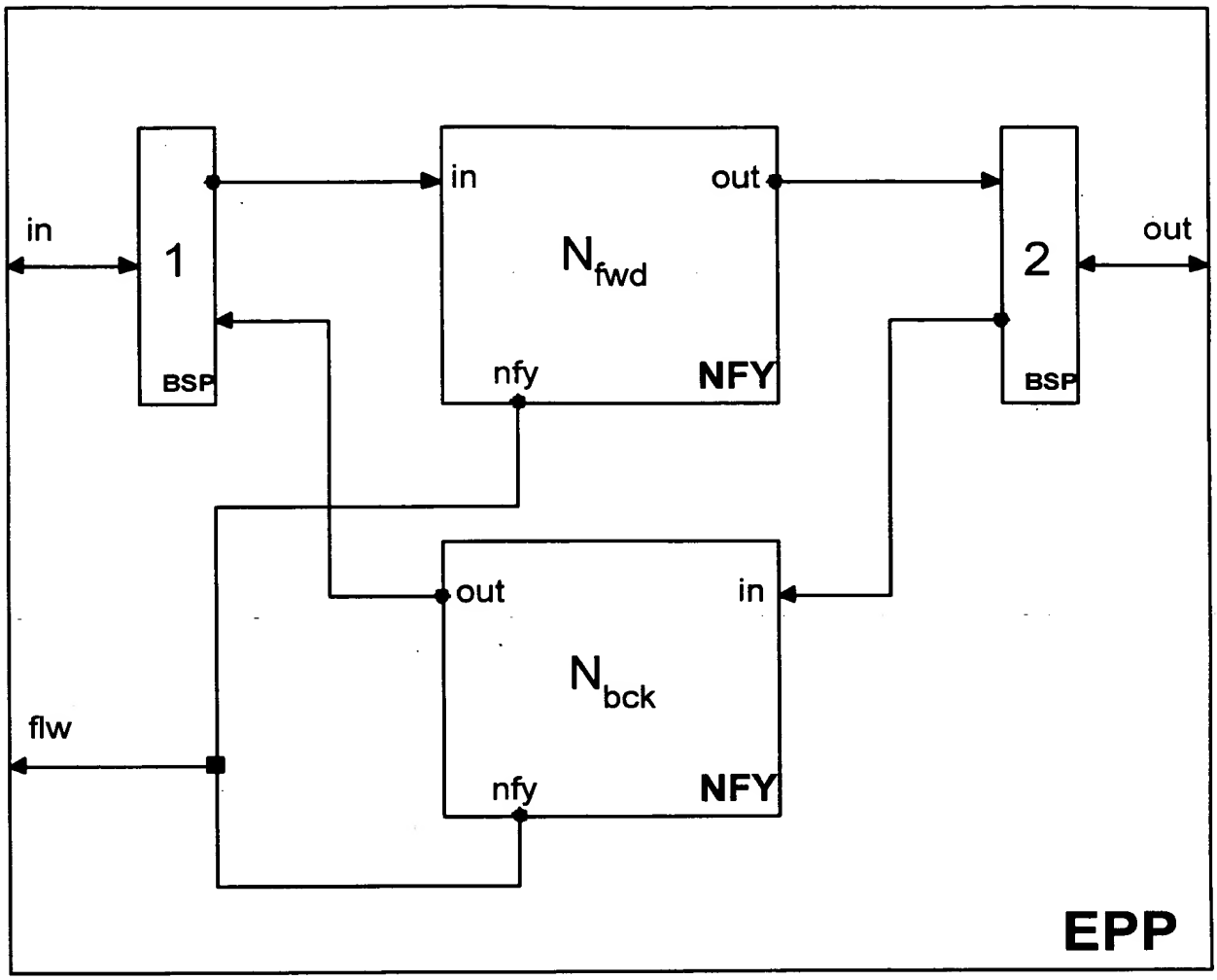


Fig. 123

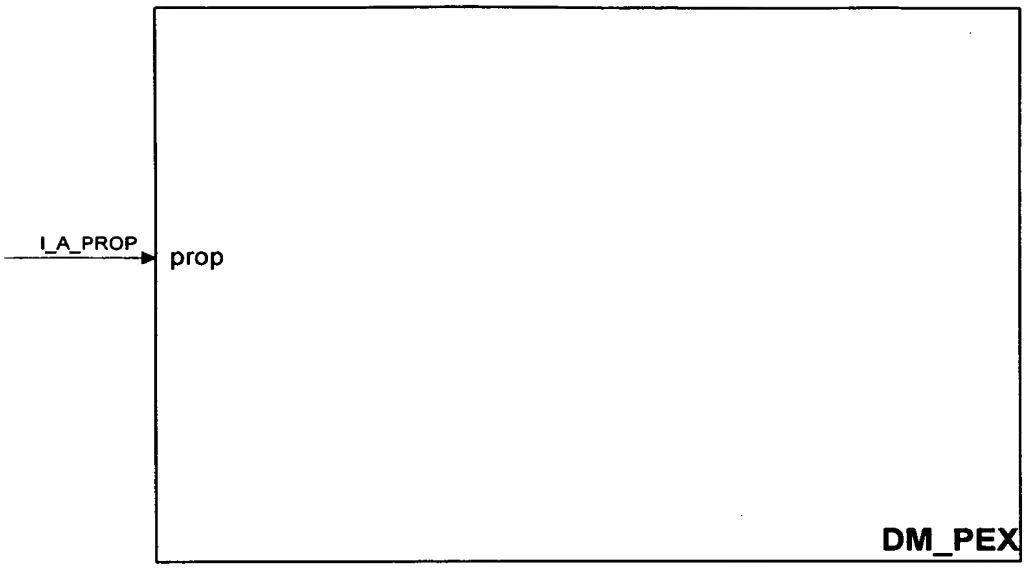


Fig. 124

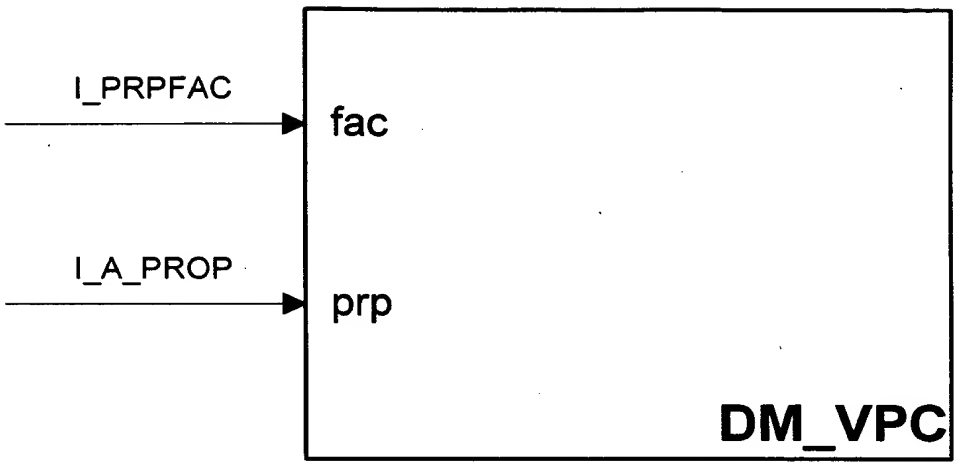


Fig. 125

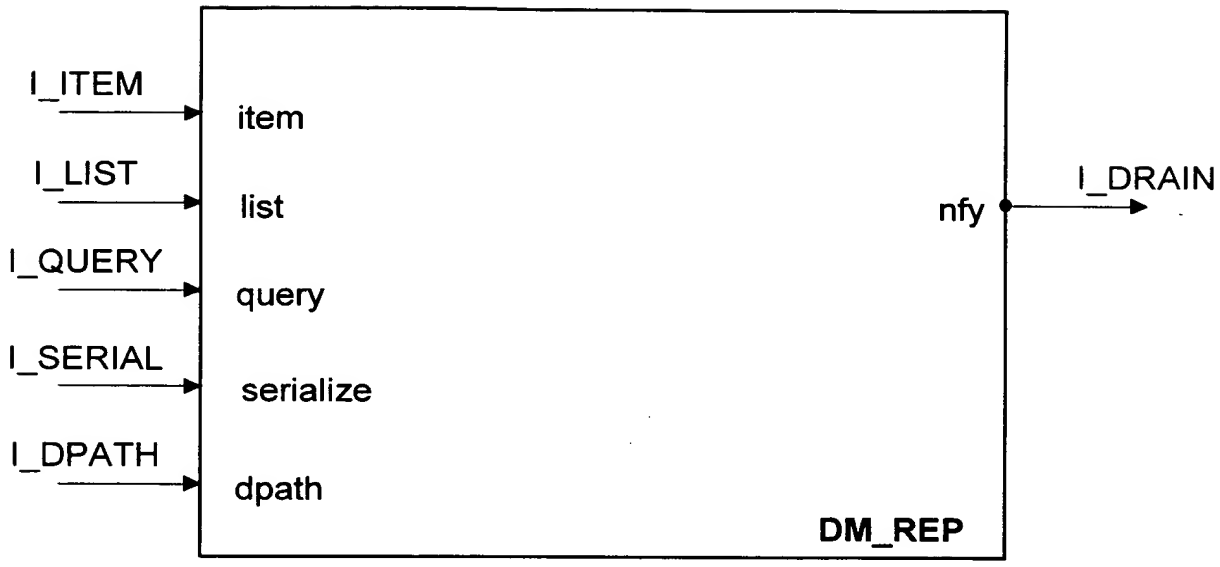

I_ITEM
item
I_LIST
list
I_QUERY
query
I_SERIAL
serialize
I_DPATH
dpath
nfy
I_DRAIN
DM_REP

Fig. 126

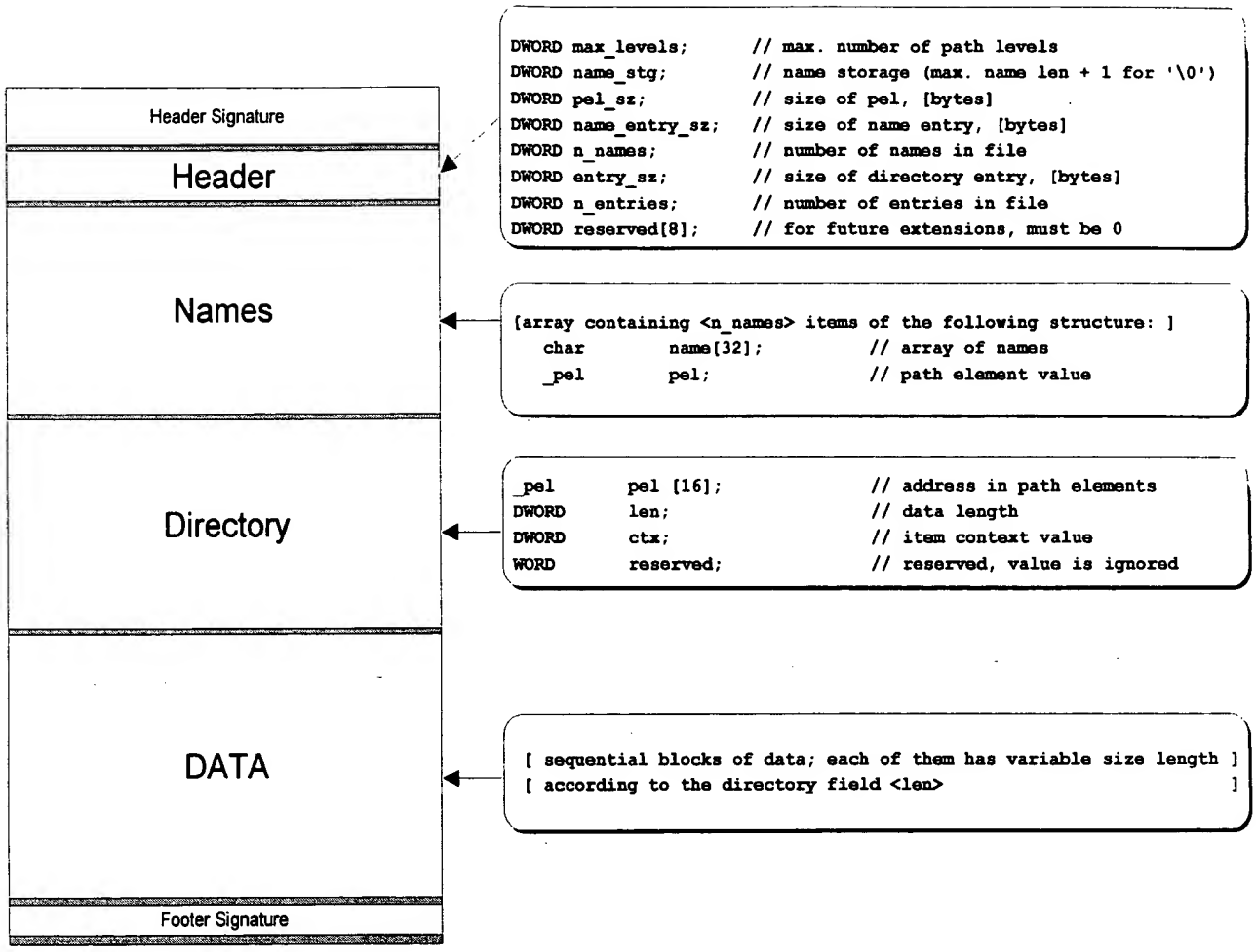

Header Signature
Header
Names
Directory
DATA
Footer Signature
DWORD max_levels; // max. number of path levels
DWORD name_stg; // name storage (max. name len + 1 for '\0')
DWORD pel_sz; // size of pel, [bytes]
DWORD name_entry_sz; // size of name entry, [bytes]
DWORD n_names; // number of names in file
DWORD entry_sz; // size of directory entry, [bytes]
DWORD n_entries; // number of entries in file
DWORD reserved[8]; // for future extensions, must be 0
[array containing <n_names> items of the following structure:]
char name[32]; // array of names
_pel pel; // path element value
_pel pel [16]; // address in path elements
DWORD len; // data length
DWORD ctx; // item context value
WORD reserved; // reserved, value is ignored
[sequential blocks of data; each of them has variable size length]
[according to the directory field <len>]

Fig. 127

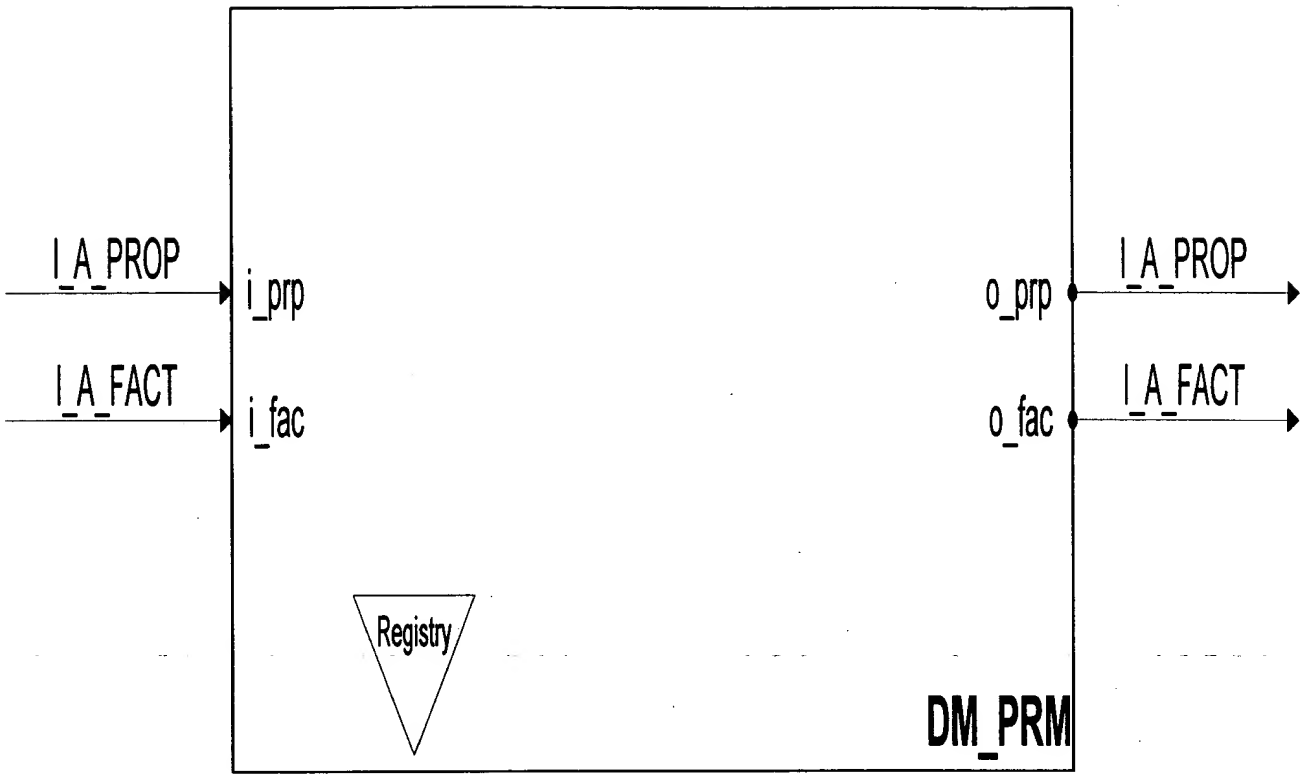

I_A_PROP
i_prp
I_A_FACT
i_fac
Registry
o_prp
o_fac
I_A_PROP
I_A_FACT
DM_PRM

Fig. 128

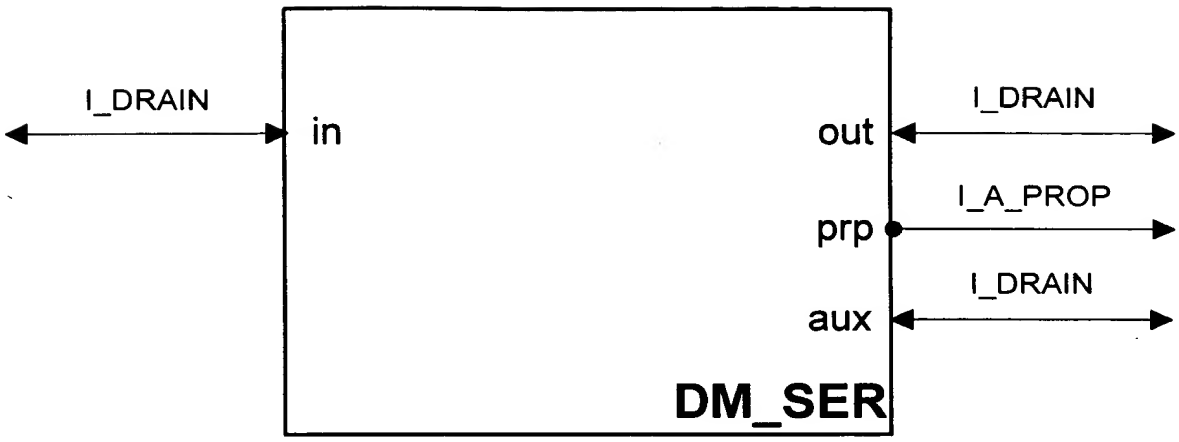


Fig. 129

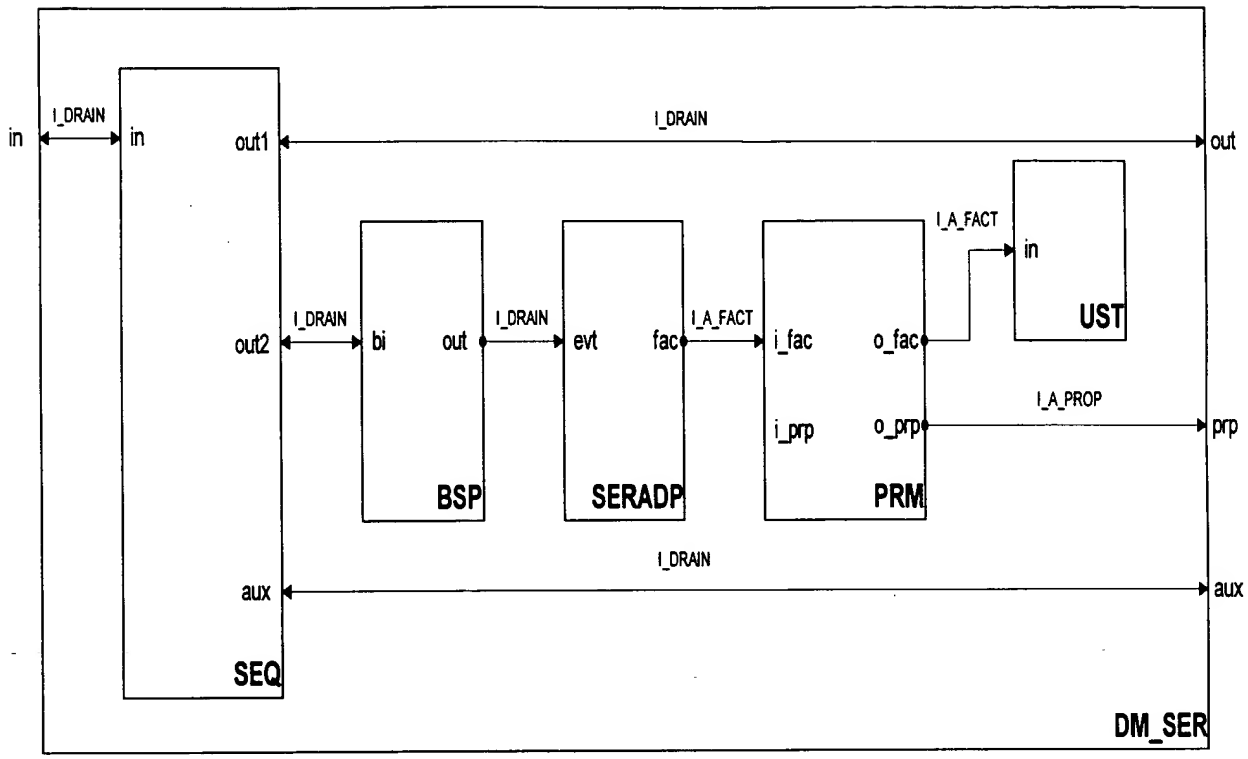

in
I_DRAIN
in
out1
I_DRAIN
out
I_A_FACT
in
UST
out2
I_DRAIN
bi
out
I_DRAIN
evt
fac
I_A_FACT
i_fac
o_fac
i_prp
o_prp
I_A_PROP
prp
BSP
SERADP
PRM
I_DRAIN
aux
aux
SEQ
DM_SER

Fig. 130

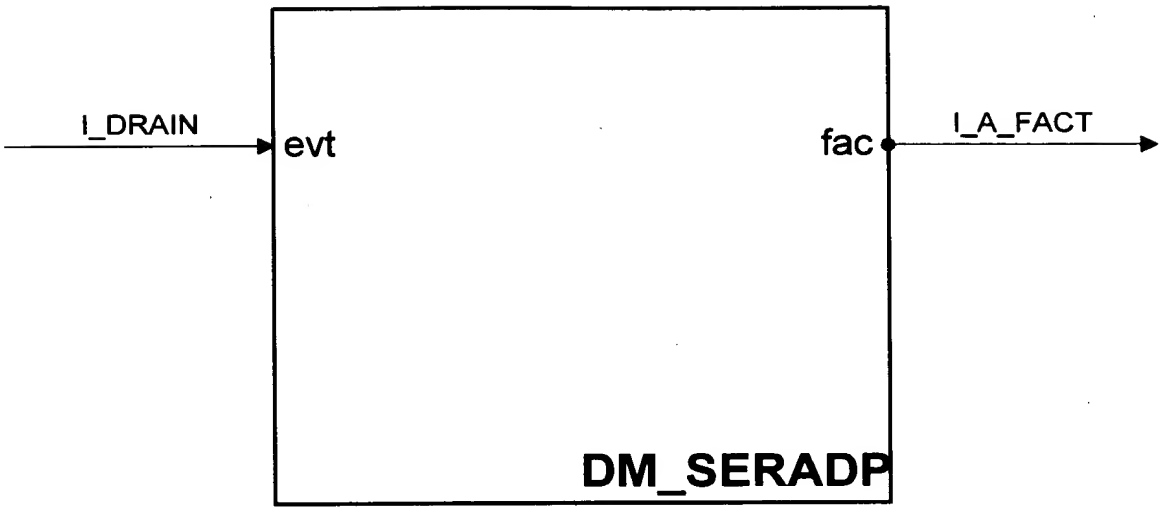


Fig. 131

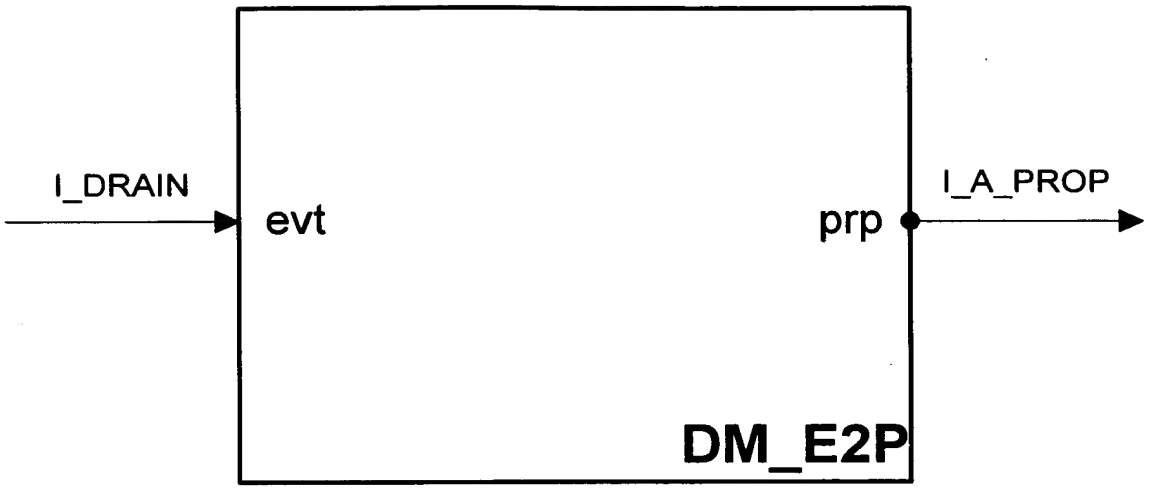


Fig. 132

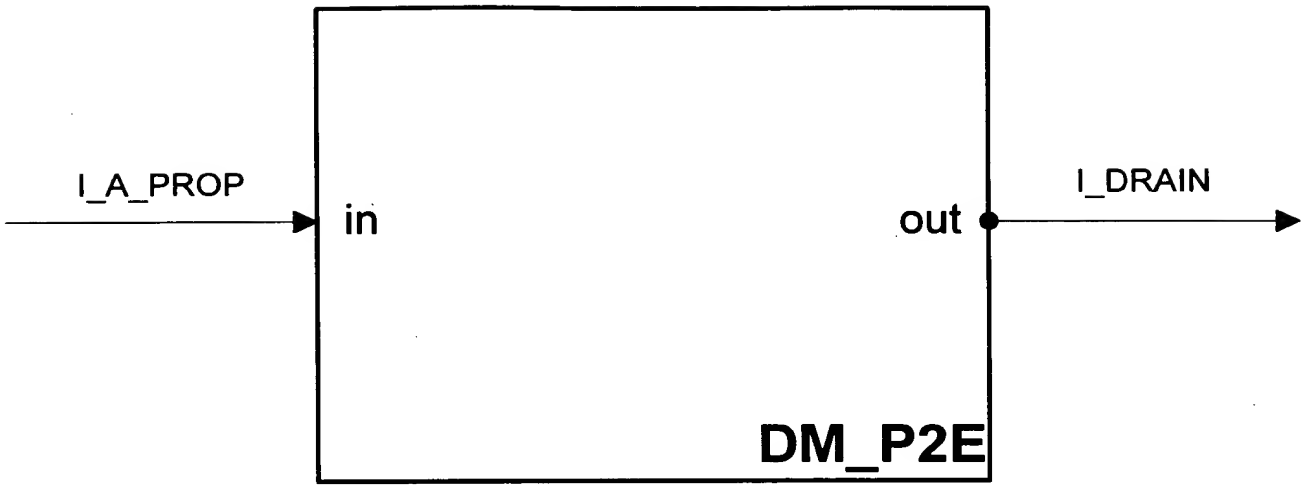


Fig. 133

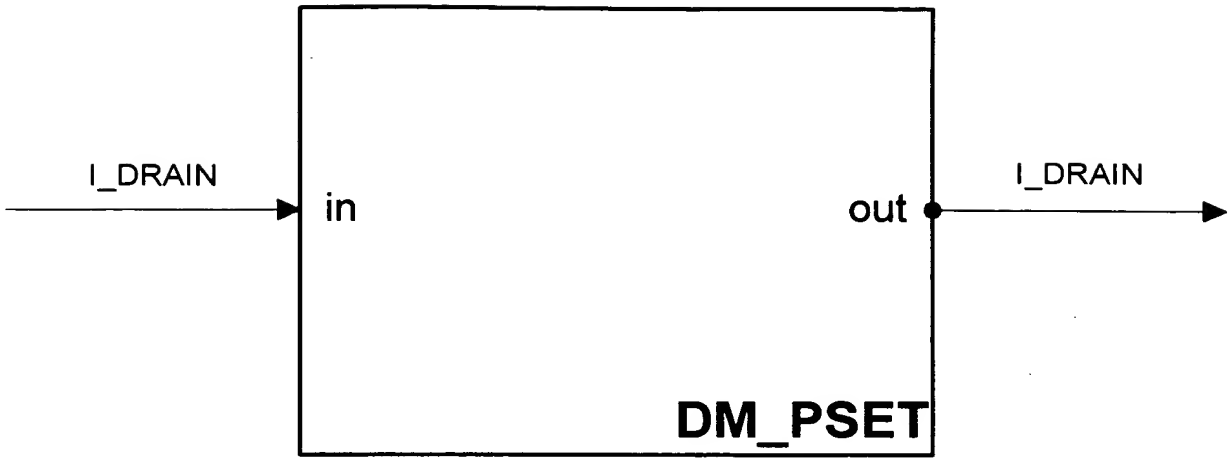


Fig. 134

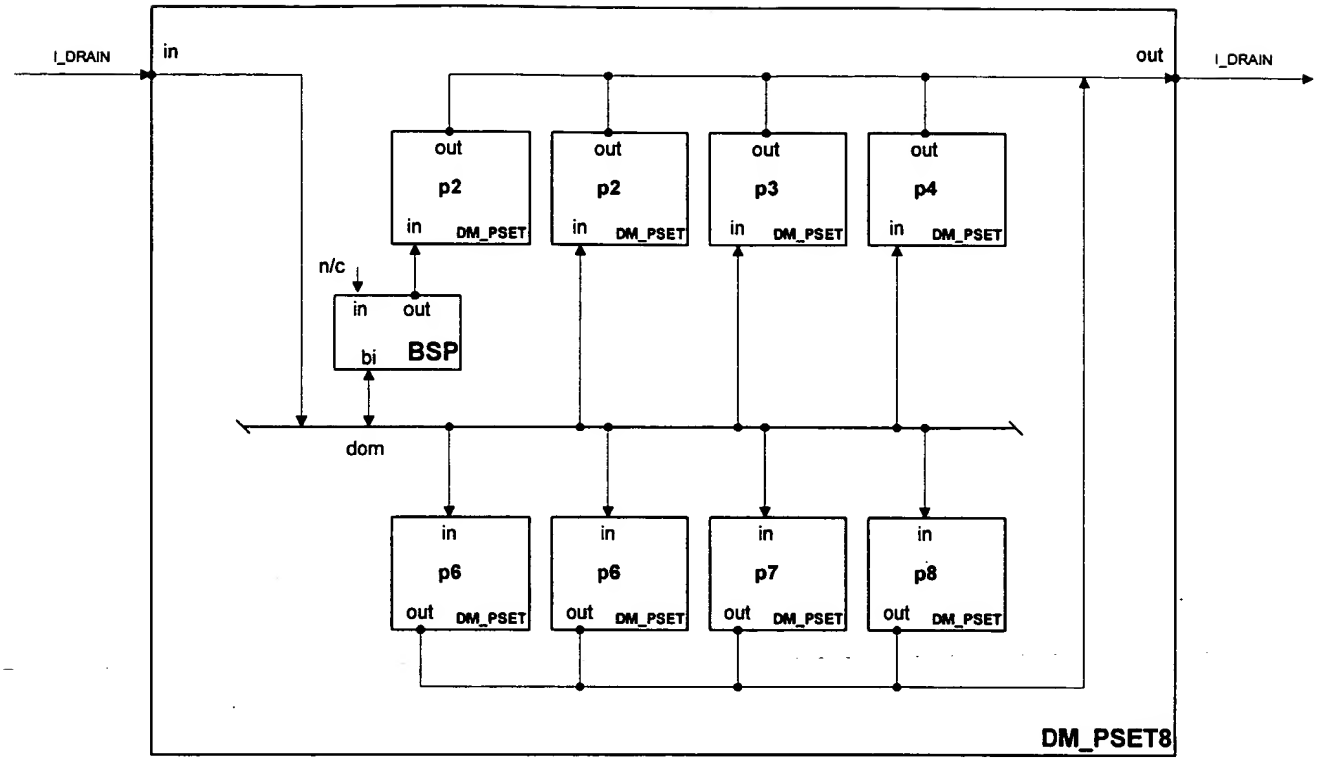

I_DRAIN
in
out
I_DRAIN
out
p2
in
DM_PSET
out
p2
in
DM_PSET
out
p3
in
DM_PSET
out
p4
in
DM_PSET
n/c
in
out
bi
BSP
dom
in
p6
out
DM_PSET
in
p6
out
DM_PSET
in
p7
out
DM_PSET
in
p8
out
DM_PSET
DM_PSET8

Fig. 135

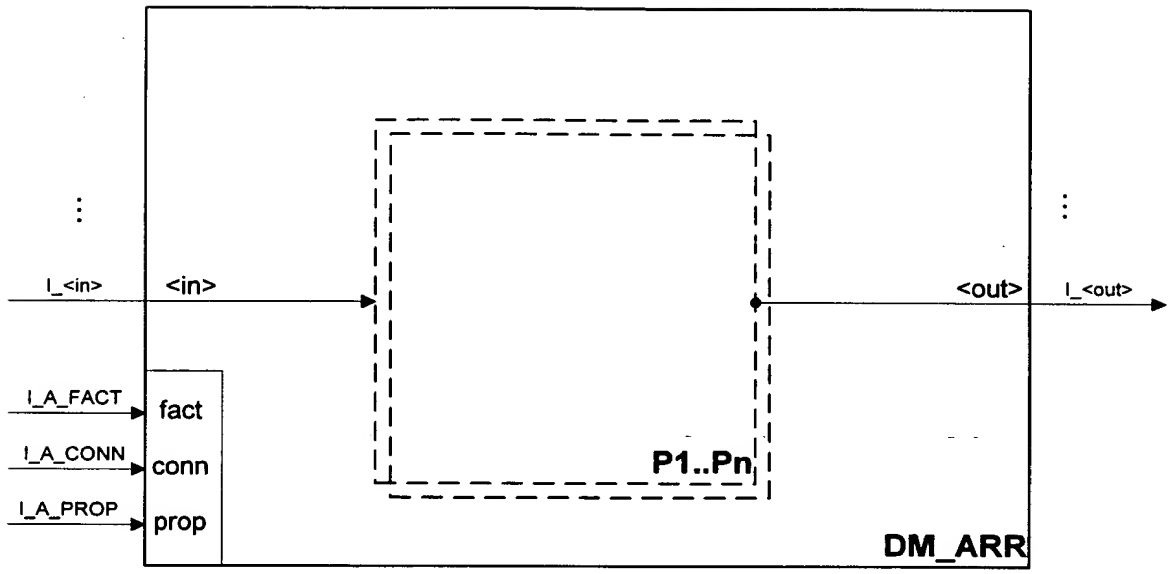

I_<in>
<in>
<out>
I_<out>
I_A_FACT
fact
I_A_CONN
conn
I_A_PROP
prop
P1..Pn
DM_ARR

Fig. 136

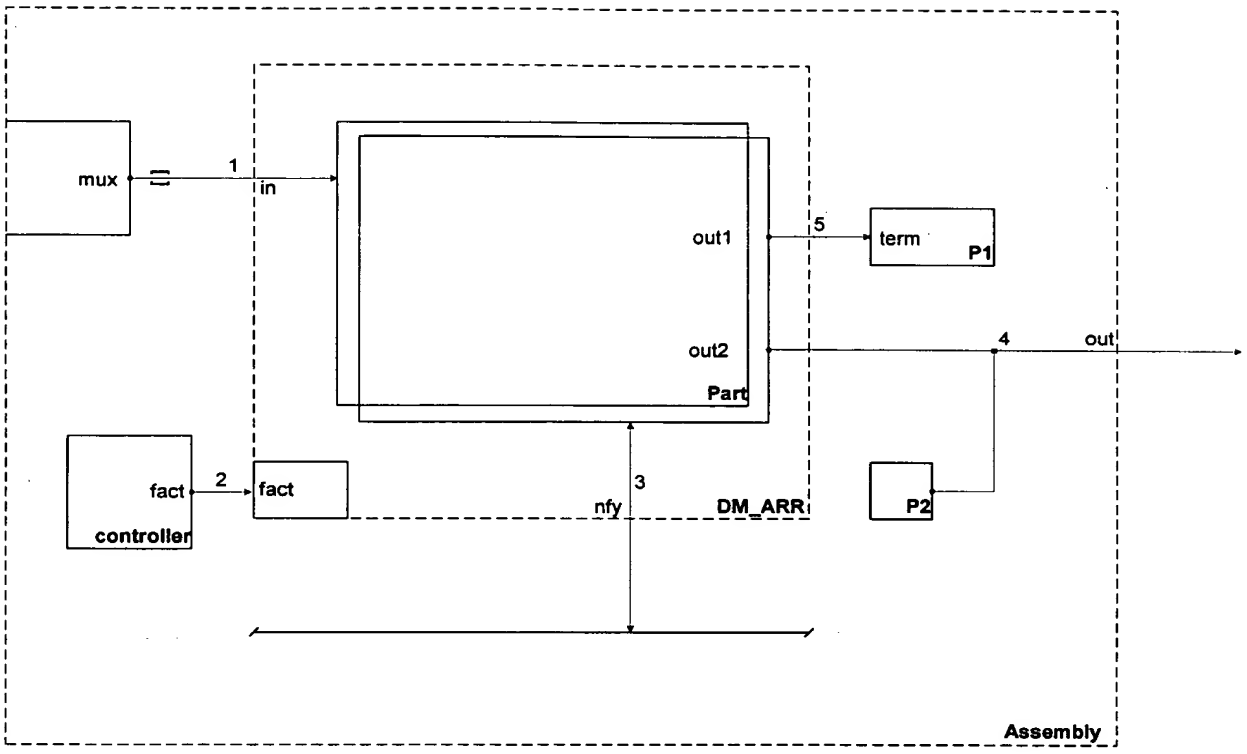

mux
1
in
out1
5
term
P1
out2
4
out
Part
fact
2
fact
3
nfy
DM_ARR
P2
controller
Assembly

Fig. 137

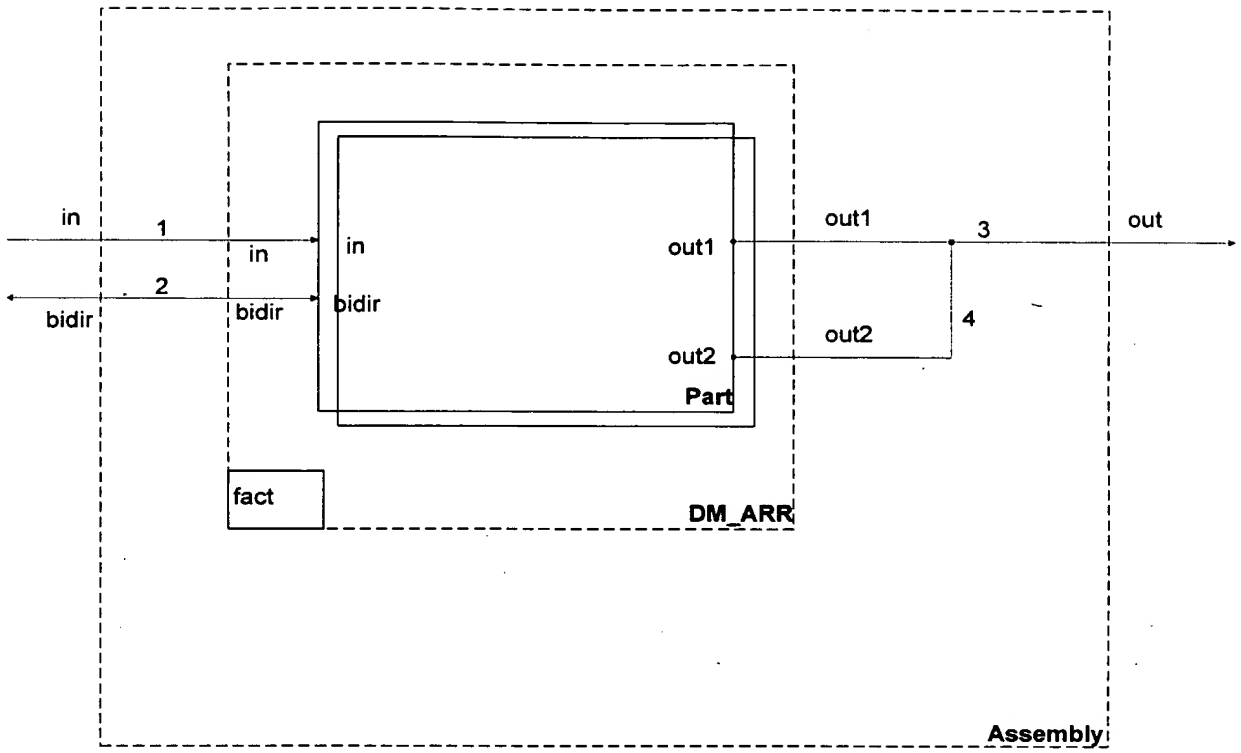

in
1
in
in
out1
out1
3
out
2
bidir
bidir
bidir
out2
4
out2
Part
fact
DM_ARR
Assembly

Fig. 138

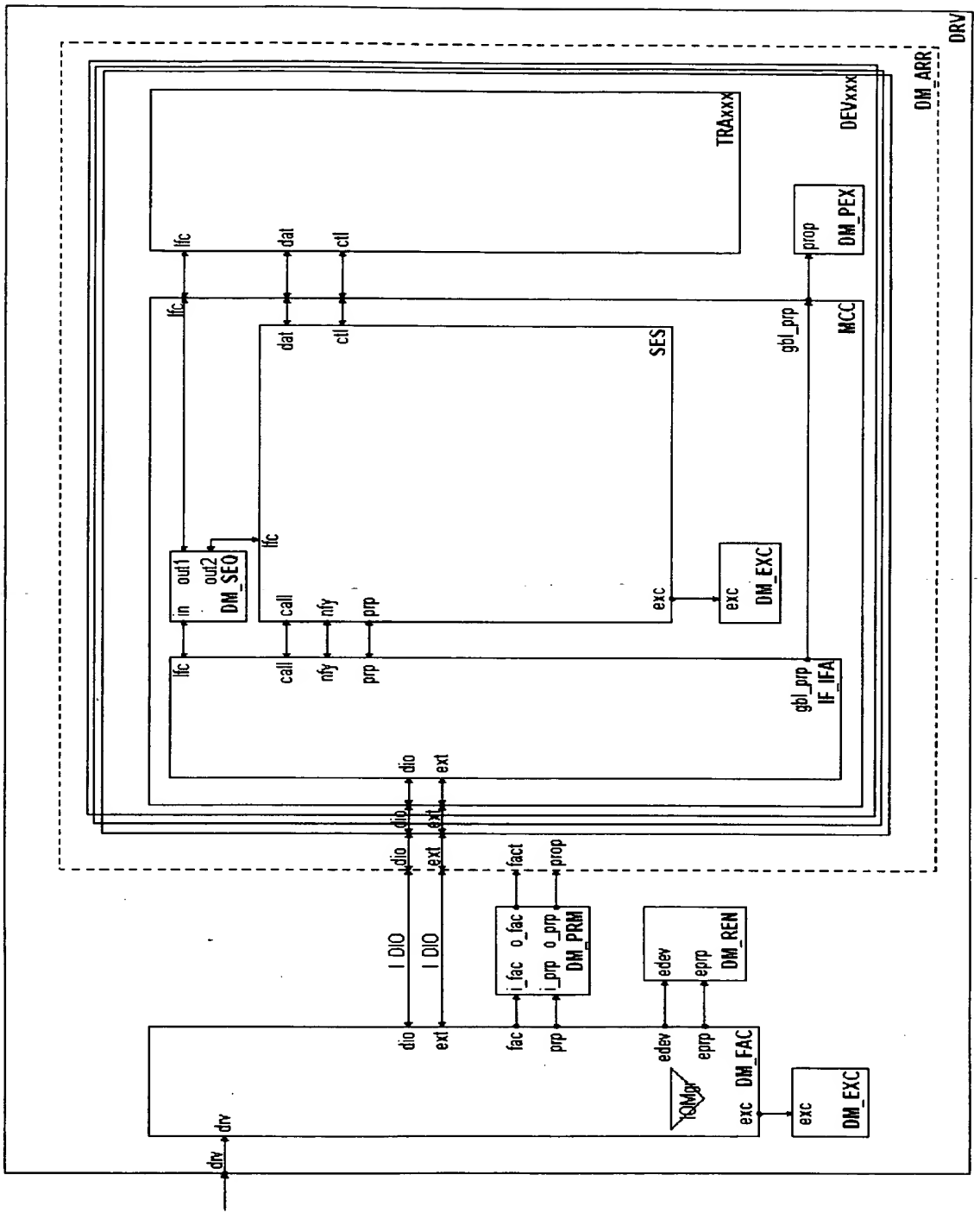

DRV
DM_ARR
TRAxxx
DEVxxx
DM_PEX
prop
ifc
dat
ctl
MCC
gbl_prp
SES
DM_SEQ
in
out1
out2
call
nfy
prp
exc
DM_EXC
IF_IFA
dio
ext
I DIO
fact
prop
DM_PRM
i_fac
o_fac
i_prp
o_prp
DM_REN
edev
eprp
fac
DM_FAC
IQMgr
drv

Fig. 139

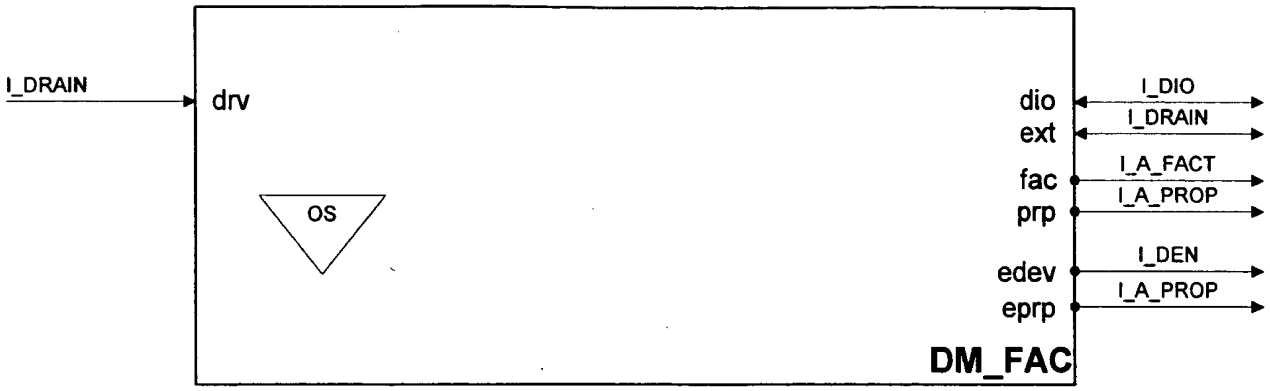

I_DRAIN
drv
OS
dio
ext
fac
prp
edev
eprp
DM_FAC
I_DIO
I_DRAIN
I_A_FACT
I_A_PROP
I_DEN
I_A_PROP

Fig. 140

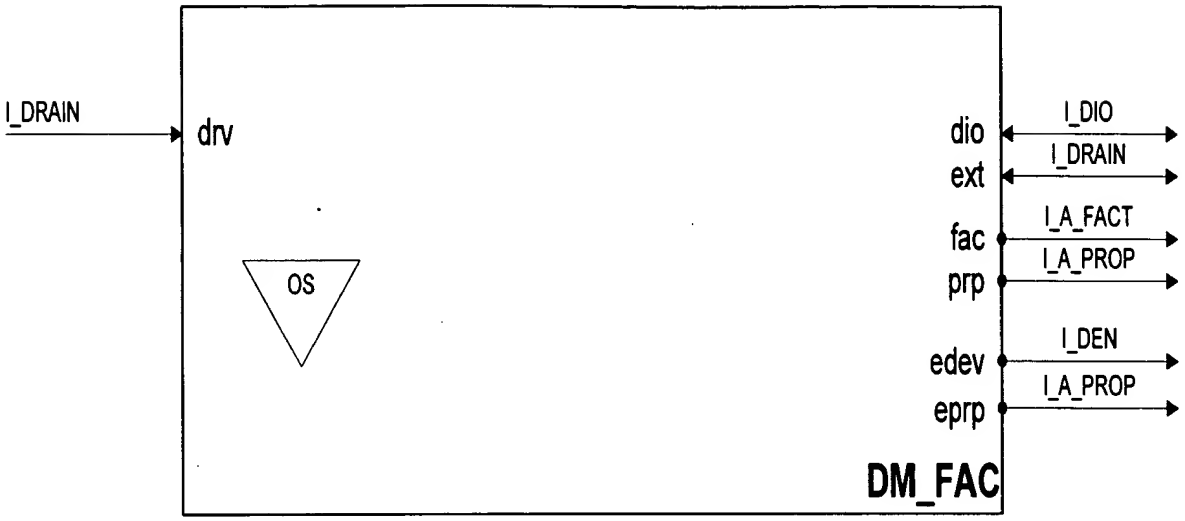

I_DRAIN
drv
OS
dio
ext
fac
prp
edev
eprp
DM_FAC
I_DIO
I_DRAIN
I_A_FACT
I_A_PROP
I_DEN
I_A_PROP

Fig. 141

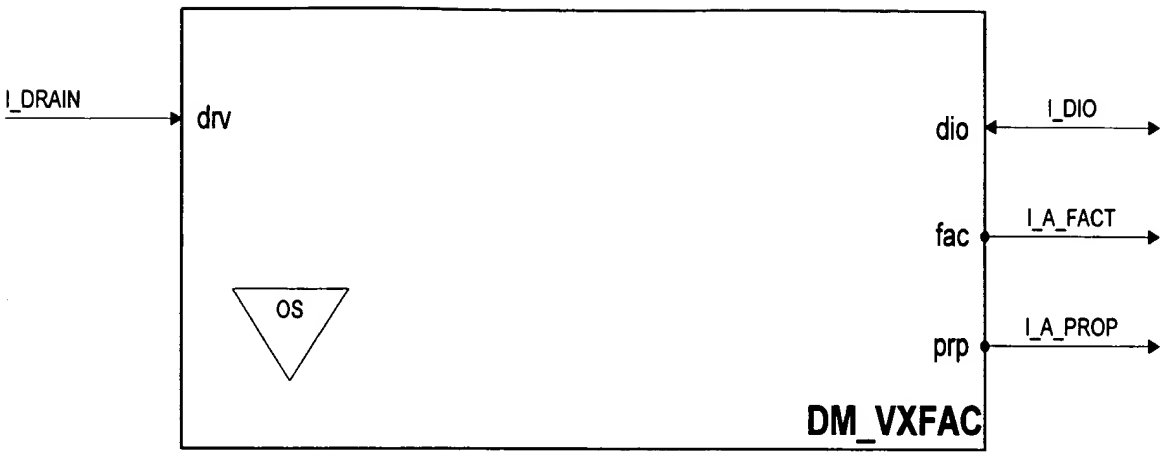


Fig. 142

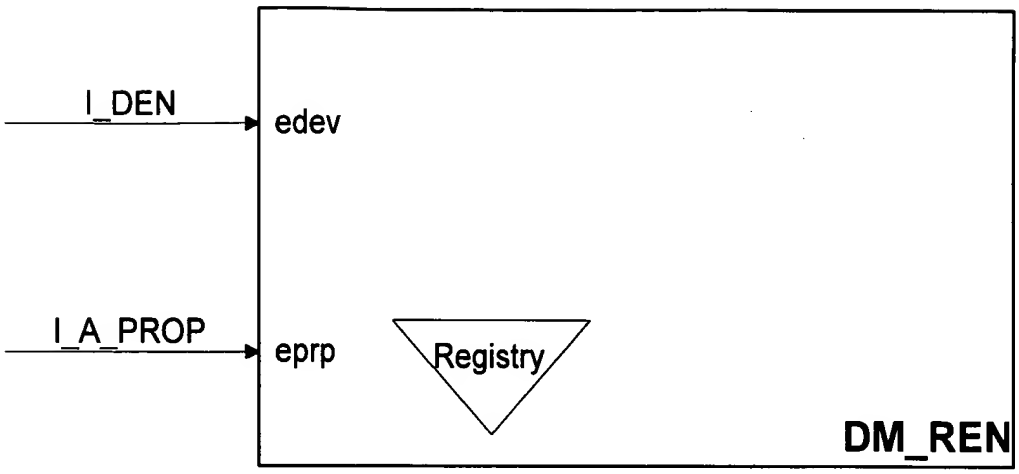


Fig. 143

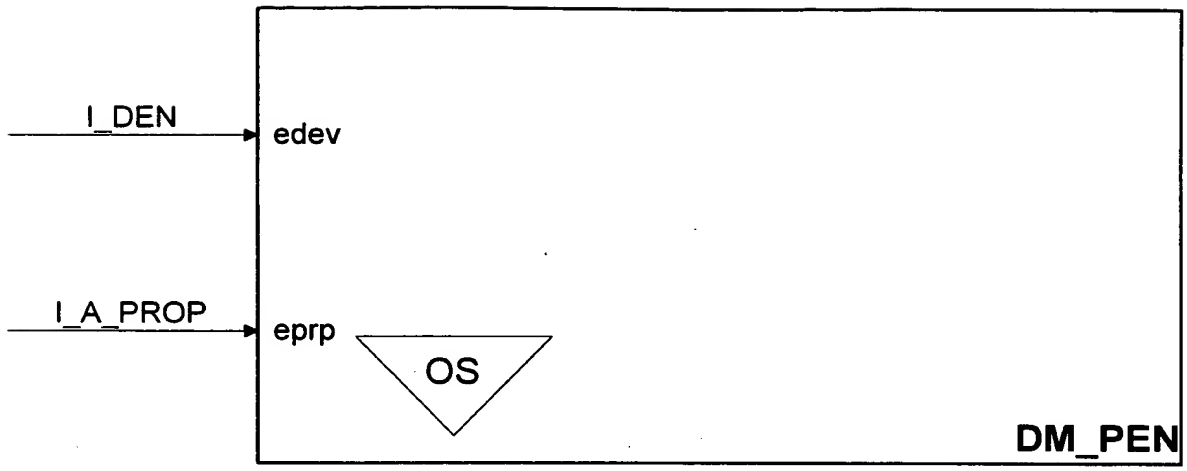


Fig. 144

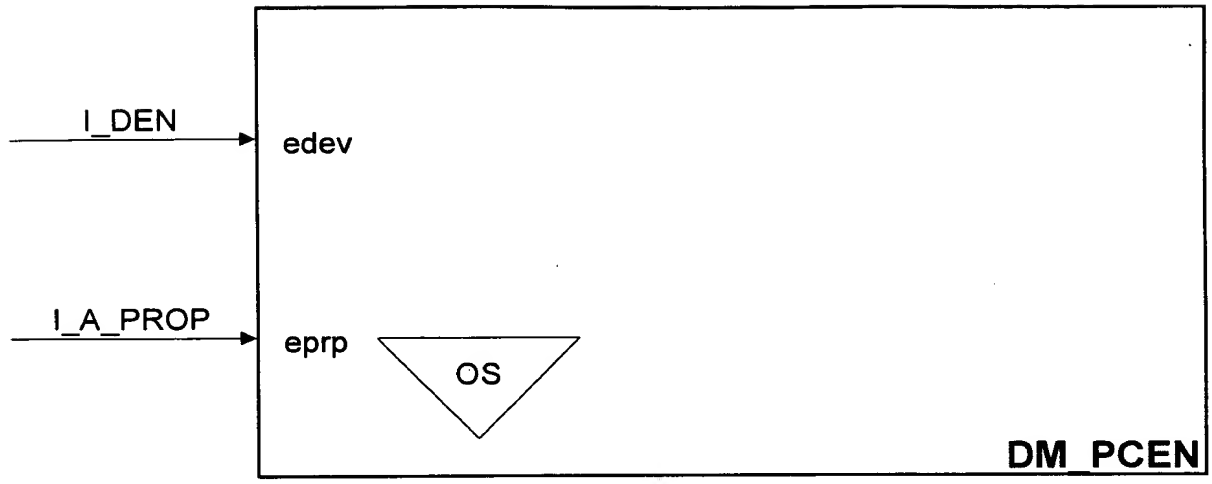


Fig. 145

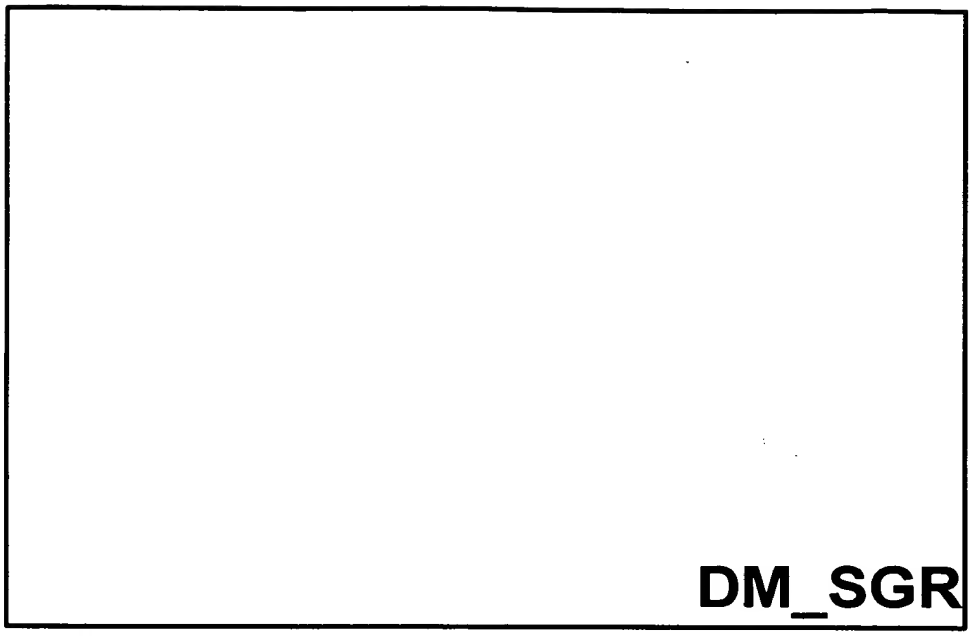


Fig. 146

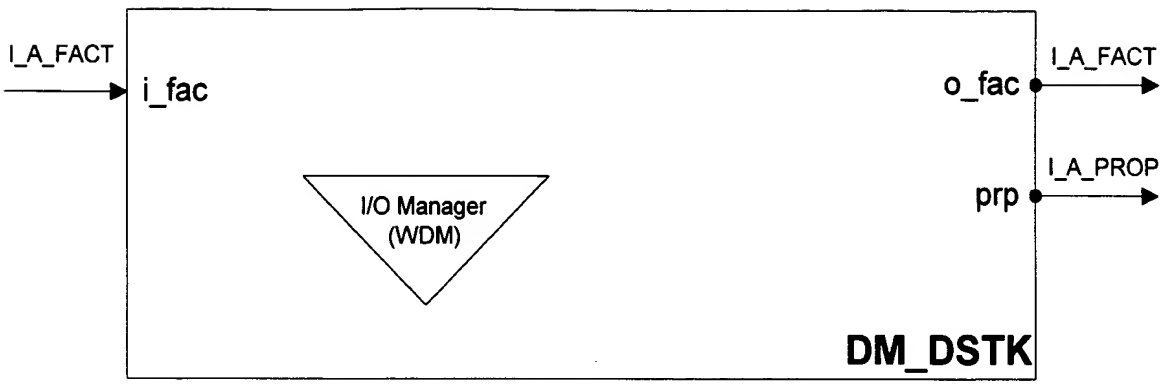


Fig. 147

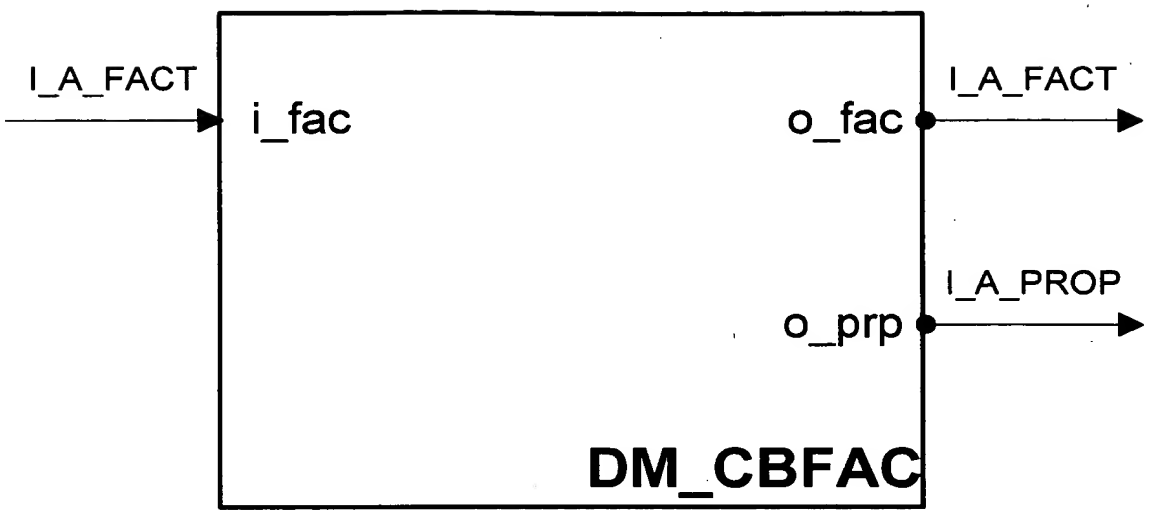
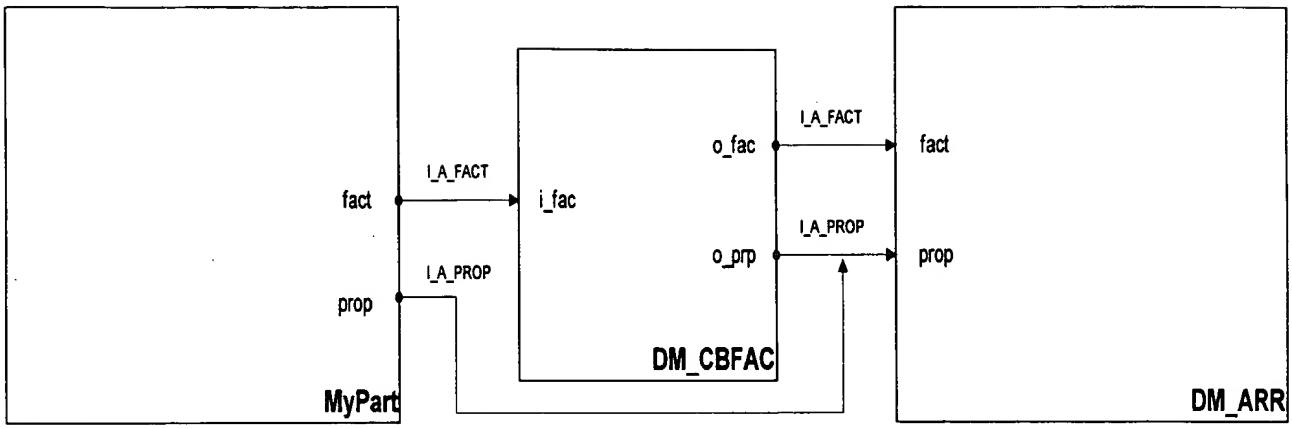


Fig. 148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fact
prop
DM_ARR

Fig. 149

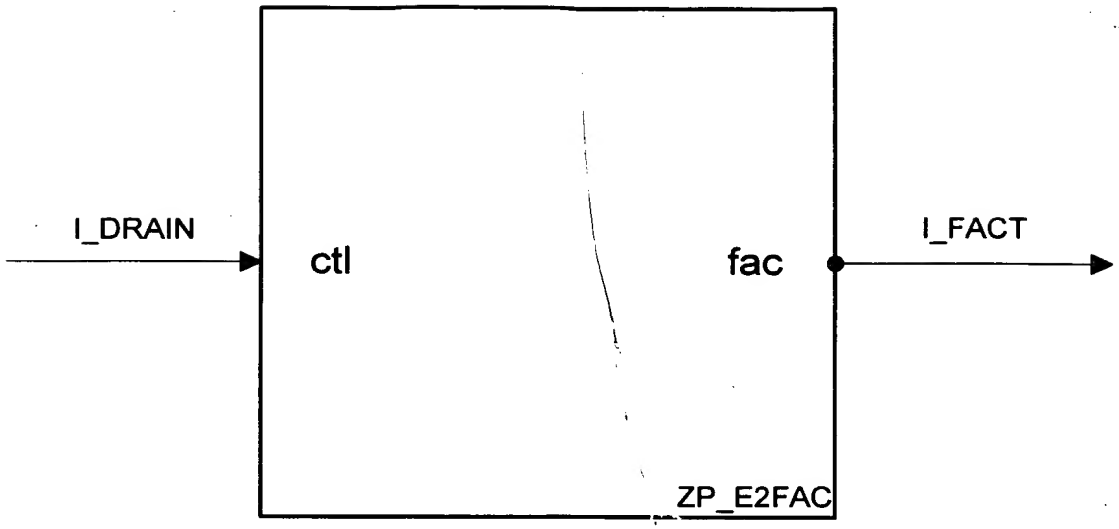

Fig. 150